VITA: Variation-Aware Interconnect Timing Analysis for Symmetric and Skewed Sources of Variation Considering Variational Ramp Input

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Abstract

As technology scales down, timing verification of digital integrated circuits becomes an extremely difficult task due to statistical variations in the gate and wire delays. Statistical timing analysis techniques are being developed to tackle this important problem. In this paper, we propose a new framework for handling variation-aware interconnect timing analysis in which the sources of variation may have symmetric or skewed distributions. To achieve this goal, we express the resistance and capacitance of a line in canonical first order forms and then use these to compute the circuit moments. The variational moments are subsequently used to compute the interconnect delay and slew at each node of an *RC* tree. For this step, we combine known closed-form delay metrics such as Elmore and AWE-based algorithms to take advantage of the efficiency of the first category and the accuracy of the second. Experimental results show an average error of 2% for interconnect delay and slew with respect to SPICE-based Monte Carlo simulations.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids.

General Terms

Algorithms, Measurement, Performance, Design, Sensitivity.

Keywords

Statistical timing analysis, Elmore delay, Moment calculation, sources of variation.

1. Introduction

Process technology and operating condition induced variability of gates and wires in VLSI circuits makes timing analysis of such circuits a challenging task [1]. As the number of sources of variations increases, it is impossible to perform static timing analysis to analyze all corners [3]. Furthermore, the identification of the corner-point is a complicated task, which is dependent on the precise interconnect and gate structure [4]. Statistical timing analysis (denoted by σTA) provides an effective solution to this important and complex problem [1][3].

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σTA approaches can be classified into two groups: path-based and block-based. Because of the high computational complexity associated with the path-based σTA, block-based σTA has received a lot of attention. In block-based σTA, every timing quantity of interest (e.g., delay and slew, arrival time and required arrival time) is represented as a function of global sources of variation (denoted by X_i) and independent random sources of variation (denoted by S_i) in the canonical first-order (denoted by CFO) form [3]. As with its STA counterpart, block-based σTA breaks the analysis into two parts: 1) variational interconnect timing analysis and 2) variational gate timing analysis. In this work, we focus on the variation-aware interconnect timing analysis.

Interconnect timing analysis in STA has been widely studied. It is well established that the Elmore delay metric [4] (which uses the first moment of the impulse response transfer function) can be off by orders of magnitude in some cases. To address the accuracy problem, different delay metrics have been proposed [6]-[8]. For example, the empirical D2M metric [6] uses the first two moments of the impulse response transfer function. Similarly, in [9], we described a new approach (called TFA) to find the interconnect delay and slew by using two moments of the impulse response. AWE methods are based on a variable refinement waveform estimator for approximating a generalized linear *RLC* interconnect. The AWE-based interconnect analysis tools (e.g., RICE [10], PRIMA [11]), which use the higher order moments of the impulse response to approximate poles of the circuit, produce the time-domain waveform of the output under arbitrary inputs. As a result, these techniques exhibit high accuracy. In spite of this, the Elmore delay metric continues to be used for interconnect delay calculation during the various steps of the physical design because of its high efficiency.

For interconnect timing analysis in σTA, the authors in [2] express the resistance and capacitance of an interconnect line as a linear function of random variables and then use these r.v.'s to compute the circuit moments. These variability-aware moments are used in standard closed-form delay metrics such as the Elmore metric to compute interconnect delay *PDF*'s. Unfortunately, this method can produce erroneous results due to the inaccuracy of the closed-form delay metrics. In addition, the authors do not provide a solution for the case of non-symmetric distribution of different sources of variations. On the other hand, resorting to AWE-based approaches to evaluate sensitivity of the interconnect delay and output slew to the sources of variations is seemingly impractical. Therefore, in this paper, we present Variation-Aware Interconnect Timing Analysis method (named VITA, which comprises of the following steps):

1) Given the variational resistive-capacitive load and the variational ramp input (where all resistances and capacitances and

the input are represented in the CFO form), an efficient algorithm is employed to calculate variation-aware circuit moments in the CFO form.

2) Plugging these variational circuit moments in any of the existing closed-form delay metrics such as Elmore and also by introducing a set of new linearization techniques, interconnect delay and slew in the CFO form are calculated.

3) By combining the result of the variation-aware closed-form delay metrics (as obtained in step 2) with the result of AWE-based algorithm for the nominal case of the circuit parameters, we calculate interconnect delay and slew for each node of the RC tree in the CFO form.

The remainder of this paper is organized as follows. In section 2, we review the background of the block-based σTA. Variation-aware delay and slew calculations are presented in section 3. Section 4 gives an improvement on the delay and slew obtained in section 3 by calculating the nominal delay and slew with AWE-based algorithm. Section 5 presents experimental results. Conclusions are given in section 6.

2. Background for Block-Based σTA

2.1 CFO model for timing parameters

A first-order variational model is employed for all timing quantities such as the gate and wire delays, arrival times, required arrival times, slacks and slews, i.e., all timing quantities are expressed in the CFO form as:

$$A = a_{nom} + \sum_{i=1}^{m} a_i \Delta X_i + a_{m+1}\Delta S_a = a_{nom}\left(1 + \sum_{i=1}^{m} \frac{a_i}{a_{nom}}\Delta X_i + \frac{a_{m+1}}{a_{nom}}\Delta S_a\right) \quad (1)$$

where a_{nom} is the mean or the nominal value; ΔX_i's represent the variation of m global sources of variation, X_i, from their nominal values, a_i's denote the sensitivities to each of the global sources of variation, ΔS_a is the variation of independent random variable S_a, and a_{m+1} is the sensitivity of the timing quantity to S_a. By appropriately scaling the sensitivity coefficients, and without loss of generality, we may assume that ΔX_i and ΔS_a are distributions with zero mean (μ=0), variance of one (σ=1), and a pre-determined skewness [14]; i.e. *Dist*(μ=0, σ=1, *skewness*). Moreover, we define a_i/a_{nom} as the *normalized sensitivity coefficient* (denoted by NSC.)

2.2 CFO model for electrical parameters

Variation of the circuit parameters causes change in the resistance and capacitance of the wire, thereby, making the wire delay and slew to vary accordingly. Therefore, we need to capture the effect of variations on the electrical parameters. Classifying the sources of variation into global and independent random sources of variation, we represent electrical parameters of the wire (i.e., R and C) in the CFO form. For instance, R and C in the CFO form are calculated as follows [12]:

$$R = R_{nom} + \sum_{i=1}^{m} r_i \Delta X_i + r_{m+1}\Delta S_r \qquad C = C_{nom} + \sum_{i=1}^{m} c_i \Delta X_i + c_{m+1}\Delta S_c \quad (2)$$

where R_{nom} and C_{nom} represent nominal resistance and capacitance values, computed when the sources of variation are at their nominal or typical values.

2.3 Converting into CFO form

As mentioned in sections 2.1 and 2.2, it is important to represent timing and electrical quantities in the CFO form. This in turn enables one to propagate first order sensitivities to different sources of variation through the circuit timing graph [3][12]. In addition, it makes statistical computations efficient and practical and provides timing diagnostics with a small cost in terms of the cpu time.

A key question is how to convert some quantity of interest (which itself is a function of CFO variables) into the CFO form. First, however, we explain how to calculate a number of arithmetic operations (i.e., addition, subtraction, multiplication, division, and square root) on two CFO operands. These operations will be subsequently utilized during interconnect timing analysis in order to put the result in the CFO form.

Suppose A and B are two parameters in CFO form:

$$A = a_{nom} + \sum_{i=1}^{m} a_i \Delta X_i + a_{m+1}\Delta S_a \qquad B = b_{nom} + \sum_{i=1}^{m} b_i \Delta X_i + b_{m+1}\Delta S_b \quad (3)$$

We represent the results of the operations on these two operands in CFO form below. In each case, the results expression was obtain in such a way that the first and second moments of the approximated output in CFO form are equal to the first and second moments of the actual (exact) result.

Addition and subtraction- If $C=A\pm B$, then C in CFO form can be written as:

$$C = A \pm B = (a_{nom} \pm b_{nom}) + \sum_{i=1}^{m} (a_i \pm b_i)\Delta X_i + \sqrt{a_{m+1}^{\ 2} + b_{m+1}^{\ 2}}\,\Delta S_c \quad (4)$$

Multiplication- If $C=A\times B$, then C in the CFO form can be written as:

$$C = A \times B = a_{nom}b_{nom} + \sum_{i=1}^{m} (a_{nom}b_i + a_i b_{nom})\Delta X_i + \sum_{i=1}^{m} a_i b_i \Delta X_i^{\ 2} + \sqrt{(a_{nom}b_{m+1})^2 + (a_{m+1}b_{nom})^2}\,\Delta S_c \quad (5)$$

However, because of the nonlinear term, Equation (5) is not in the CFO form. To put it in CFO form, we use the following linearization technique. The ΔX_i^2 is substituted with a linear approximation $\mu+\sigma\Delta X_i$, such that the first and second moments of the actual term and the approximated term are equal i.e.,

$$E(\Delta X_i^{\ 2}) = E(\mu + \sigma\Delta X_i) \qquad E(\Delta X_i^{\ 4}) = E\left\{(\mu + \sigma\Delta X_i)^2\right\} \quad (6)$$

Consequently, C in CFO form can be approximated as:

$$C \cong \left(a_{nom}b_{nom} + \mu\sum_{i=1}^{m} a_i b_i\right) + \sum_{i=1}^{m} (a_{nom}b_i + a_i b_{nom} + a_i b_i \sigma)\Delta X_i + \sqrt{(a_{nom}b_{m+1})^2 + (a_{m+1}b_{nom})^2}\,\Delta S_c \quad (7)$$

For instance, if ΔX_i is a unit normal distribution $N(\alpha=0, \beta=1)$, thus;

$$E(\Delta X_i^{\ 2}) = \alpha^2 + \beta^2 \qquad E(\Delta X_i^{\ 4}) = \alpha^4 + 6\alpha^2\beta^2 + 3\beta^4 \quad (8)$$

Hence, using equations (6) and (8), we have:

$$\Delta X_i^{\ 2} \cong 1 + \sqrt{2}\Delta X_i \quad (9)$$

Division- Suppose A and B are in CFO forms. The objective is to find C in CFO form while

$$C \cong \frac{A}{B} \quad \Rightarrow \quad A \cong C.B \tag{10}$$

Following the derivation for the multiplication operation, we can find the unknown coefficients of C in the CFO form.

Square root- Having A in the CFO form, the objective is to find C in the CFO form while

$$C \cong \sqrt{A} \quad \Rightarrow \quad C^2 \cong A \tag{11}$$

With the approach similar to that adopted for the multiplication operation, we can find C in the CFO form.

3. Interconnect Timing Analysis for an RC Tree in Block-Based σTA

Elmore [4] showed the delay of an *RC* tree may be approximated by using the first moment of the impulse response transfer function (i.e., -m1.) It has also been shown that the interconnect propagation delay and slew for an *RC* circuit driven by a ramp input by using the Elmore delay metric can be calculated as:

$$T_{x(\alpha\%-\beta\%)} = \sqrt{\left(T_{in(\alpha\%-\beta\%)}\right)^2 + \left(-m_1 \times \ln(\frac{100-\alpha}{100-\beta})\right)^2} \tag{12}$$

$$delay = T_{x(0\%-50\%)} - T_{in(0\%-50\%)} = \sqrt{\left(\frac{T_r}{2}\right)^2 + \left(-m_1 \times \ln(2)\right)^2} - \frac{T_r}{2} \tag{13}$$

where $T_{in}(\alpha\%\text{-}\beta\%)$ denotes the input transition time from α% point to β%. point, $T_x(\alpha\%\text{-}\beta\%)$ is the transition time of node x from its α% point to β%. point, m1 is the first moment of the impulse response transfer function, and T_r is the input transition time form 0% point to 100% point.

D2M [6] uses two moments of the impulse response transfer function, thus yielding a more accurate delay and slew value:

$$T_{x(\alpha\%-\beta\%)} = \sqrt{\left(T_{in(\alpha\%-\beta\%)}\right)^2 + \left(\frac{m_1^2}{\sqrt{m_2}} \ln(2) \times \ln(\frac{100-\alpha}{100-\beta})\right)^2} \tag{14}$$

$$delay = T_{x(0\%-50\%)} - T_{in(0\%-50\%)} = \sqrt{\left(\frac{T_r}{2}\right)^2 + \left(\frac{m_1^2}{\sqrt{m_2}} \ln(2) \times \ln(2)\right)^2} - \frac{T_r}{2} \tag{15}$$

TFA [9] approximates the slew of an interconnect using the first two circuit moments as follows:

$$T_{x(\alpha\%-\beta\%)} = \sqrt{\left(T_{in(\alpha\%-\beta\%)}\right)^2 + \left(-m_1 \times \gamma_{\alpha\%-\beta\%}\right)^2} \tag{16}$$

where γ is a function of $m_2/{m_1}^2$. For a general second order system, when applying a step input to the system, γ is a linear function of $m_2/{m_1}^2$ and is estimated as follows:

$$\gamma_{\alpha\%-\beta\%} = \lambda_{\alpha\%-\beta\%}(\frac{m_2}{{m_1}^2}) + \kappa_{\alpha\%-\beta\%} \tag{17}$$

where

$$\gamma_{\alpha\%-\beta\%} = \gamma_{\beta\%} - \gamma_{\alpha\%}$$
$$\lambda_{\alpha\%-\beta\%} = \lambda_{\beta\%} - \lambda_{\alpha\%} \qquad \kappa_{\alpha\%-\beta\%} = \kappa_{\beta\%} - \kappa_{\alpha\%} \tag{18}$$

λ and κ values for different transition points are reported in [9].

AWE can perform highly accurate interconnect timing analysis; However, its efficiency is much lower compared to Elmore, D2M, and TFA. The efficiency issue becomes even more critical when doing variational interconnect timing analysis.

Problem statement: Given is an *RC* tree representation in a design as shown in Figure 1, where each R and C is in the CFO form and the *RC* tree is driven with a ramp input, also, in the CFO form. The objective is to calculate the voltage transition time and propagation delay from the input node to each node in the tree in the CFO form.

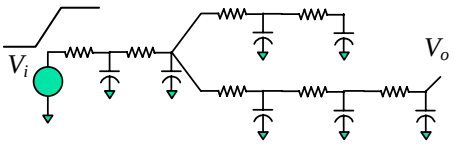

Figure 1. An *RC* tree where an input ramp voltage V_i is applied and V_o is the voltage of the output pin.

The proposed framework to solve the aforesaid problem is as follows. 1) We first compute the circuit moments in the CFO form, and 2) By using the obtained moments, we calculate the interconnect propagation delay and slew at each node of the *RC* tree in the CFO form.

3.1 Variational moment calculation in CFO form

To calculate the delay and slew of any node in an *RC* tree in CFO form, we need to first obtain the circuit moment(s) in the CFO form (Elmore metric requires the first moment only. However, D2M and TFA require the first two moments). Given is an *RC* tree representation in a design as shown in Figure 1, where each R and C is in the CFO form. The objective is to find impulse response moment(s) in CFO form.

It has been shown that circuit moments in an *RC* tree can be computed directly as functions of the *RC*s in linear time in the size of the circuit [13]. The circuit moments of an *RC* tree can be computed efficiently by path tracing. The p-th order circuit moment (p>1) of node i (m_p^i) in an *RC* tree can be expressed as:

$$m_p^i = \sum_k -R_{ik} C_k m_{p-1}^i \tag{19}$$

Here, summation is taken over all the nodes other than the source node. C_k is the capacitance at node k and R_{ik} denotes the total overlap resistance in the unique paths from the source node to the nodes i and k [13]. Since R_{ik} and C_k are in the CFO form, by using the multiplication and addition operations presented in section 2.3, we can calculate any moment in the CFO form.

3.2 Delay and slew calculation in CFO form using moments in CFO form

Given are circuit moments in CFO form. The objective is to calculate the delay and slew at each node of the RC tree in CFO form. Based on the discussion at the beginning of section 3, the delay and slew at each node of the *RC* tree can approximately be written as a function of the input transition time and circuit moments using Elmore, D2M, TFA and many other delay metrics as in Eqns. (12)-(18). Therefore, if we substitute the obtained moments from section 3.1 in those equations, and use the operations in section 2.3, we will end up computing the delay and slew of each node in CFO form.

4. A Mixed Method for Interconnect Timing Analysis for RC Tree in Block-Based σTA

Section 3 presented a method to calculate voltage transition time and interconnect delay in CFO form by using known closed form delay metrics. The proposed method was based on the circuit moments of the impulse response in the CFO form. Calculating variation-aware interconnect delay based on Elmore delay, D2M, or TFA method will cause pessimistic and possibly erroneous results. Using more accurate delay calculation algorithm such as AWE is CPU-intensive. Furthermore, as the number of sources of variations increases, interconnect delay and slew calculation become more complex. Thus, we propose an efficient and accurate *mixed method*, which benefits from the accuracy of exact algorithms such as AWE, and the efficiency of fast algorithms like Elmore, D2M or TFA. Next, we explain how to compute a more accurate, yet efficient, interconnect delay in CFO form. The discussion can be applied in the same manner to any other timing quantity (e.g., slew). Suppose the actual interconnect delay in the CFO from can be represented as follows:

$$D_{act} = d_{act,nom} + \sum_{i=1}^{m} d_{act,i}\Delta X_i + d_{act,m+1}\Delta S_d = d_{act,nom}\left(1 + \sum_{i=1}^{m} \frac{d_{act,i}}{d_{act,nom}}\Delta X_i + \frac{d_{act,m+1}}{d_{act,nom}}\Delta S_d\right) \quad (20)$$

Previously we showed how to use circuit moments of impulse response to approximately compute delay in CFO form. We define D_{apx} (in CFO form) as an approximate value for D_{act}:

$$D_{apx} = d_{apx,nom} + \sum_{i=1}^{m} d_{apx,i}\Delta X_i + d_{apx,m+1}\Delta S_d = d_{apx,nom}\left(1 + \sum_{i=1}^{m} \frac{d_{apx,i}}{d_{apx,nom}}\Delta X_i + \frac{d_{apx,m+1}}{d_{apx,nom}}\Delta S_d\right) \quad (21)$$

D_{apx} can be calculated based on different delay metrics such as Elmore, D2M or TFA. We define $d_{apx,i}/d_{apx,nom}$ and $d_{apx,i}/d_{apx,nom}$ as approximate and actual *normalized sensitivity coefficients* (denoted by NSCs), respectively. As will be seen in the experimental results section, for different delay metrics, the approximated NSCs remain nearly the same, and furthermore, they converge to their actual NSC values. Hence,

$$\frac{d_{apx,i}}{d_{apx,nom}} \cong \frac{d_{act,i}}{d_{act,nom}} \qquad 1 \le i \le m+1 \quad (22)$$

Based on the above observation, a mixed method for transition time and interconnect delay calculation comprises of the following steps.

1) Calculate D_{apx} in the CFO form (section 3), and therefore, find $d_{apx,nom}$ and $d_{apx,i}$ for $1 \le i \le m+1$.
2) Find the actual $d_{act,nom}$ by performing the AWE algorithm for the nominal conditions of the circuit.
3) By using Eqn. (22) and the results of step 1 and 2, we get

$$d_{act,i} = d_{act,nom} \times \frac{d_{apx,i}}{d_{apx,nom}} \quad \forall i, 1 \le i \le m+1$$

After finding all $d_{act,nom}$ and $d_{act,i}$, we can write D_{act} in CFO form.

5. Experimental Results

5.1 Normal sources of variation, *N*(0,1)

To assess the quality of the solution to the general problem statement in section 3, the proposed algorithm (in section 3) is applied on 1000 random *RC* ladder with 30 segments connected in series (nodes are labeled 1 to 30 from the input to the output.) The *R* and *C* values were uniformly distributed between 1-500 ohms and 1-500pF, respectively. We characterized the variations of each *R* and *C* as a function of three normal global and one normal independent random sources of variation. The total σ variation for each *R* and *C* was considered to be 15% of their nominal value. However, sensitivities of each *R* and *C* in the circuit to sources of variation were set randomly. The nominal value for the input transition time was uniformly chosen between 10ps to 300ps. Furthermore, we characterized its variation as a function of three normal global random sources and one normal independent random source of variation. The sensitivity of the input transition time to sources of variations was also set randomly, whereas the total σ variation of the input rise time was chosen to be 15% of its nominal value.

We ran HSPICE-based Monte Carlo simulation on each case of the above circuit scenarios and compared the delay and slew results with the approach explained in section 3. The results are reported in Table 1. Experimental results indicate an average error of less than 14% for different σ values when the Elmore delay metric is used for statistical timing analysis. This error goes down to an average of 10% by applying the D2M based statistical interconnect timing analysis. TFA based approach gives an even lower average error of only 7%.

In section 4, we stated that NSCs change only slightly as the delay metrics used for statistical interconnect timing analysis are changed. To verify this statement, Figure 2 provides NSC variation for Elmore, D2M, and TFA-based interconnect timing analyses with respect to their actual NSC values for nine different circuit scenarios. The figure clearly corroborates the claim. The average error is less than 2% when the approach in section 4 (i.e., mixed method, using TFA for NSC and AWE for nominal value calculation) is employed. These results are also presented in Table 1 (cf. the last column.)

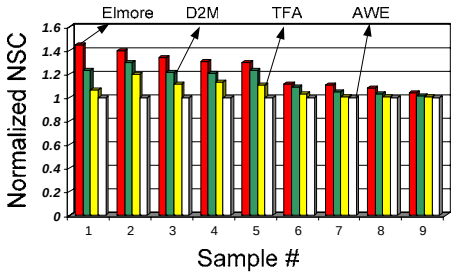

Figure 2. Changes in the normalized NSC using Elmore, D2M, TFA and AWE algorithms. Results are provided for nine different circuit scenarios.

5.2 Skewed sources of variation with μ=0, σ=1, and skew=0.5

The same set of experiments was run by using skewed sources of variation with mean of zero, variance of one, and skewness of 0.5. The average error of μ and σ for the 30-segment *RC* ladders is

presented in Table 2. Results reveal an average error of less than 15% if the Elmore delay metric is used for statistical timing analysis. This error goes down to average of 12% by applying the D2M-based statistical interconnect timing analysis. TFA-based approach gives a better average error of 9%. The average error becomes less than 3% when the mixed method (using TFA for NSC and AWE for nominal value calculation) is employed.

6. Conclusion

In this paper we presented a framework to handle the variation-aware interconnect timing analysis in block-based σTA. We expressed the resistance and capacitance of a line in a canonical first order form and used them to compute the circuit moments. These variational moments were used to compute interconnect delay and slew at each node of the *RC* tree. To achieve this goal, we combined known closed form delay metrics such as Elmore with AWE based algorithms to benefit from the efficiency of the first category as well as the accuracy of the second. Experimental results showed an average error of 2% with respect to Spice-based Monte Carlo simulation results.

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Table 1: Experimental results for *RC* ladder with normal sources of variations $N(0,1)$

Node	Elmore				D2M				TFA				Mixed (TFA+AWE)			
	Delay		Slew		Delay		Slew		Delay		Slew		Delay		Slew	
	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
10	12.3%	11.2%	13.3%	10.3%	7.3%	7.4%	7.3%	6.9%	5.3%	5.2%	4.9%	4.2%	1.9%	1.8%	1.8%	1.8%
15	11.2%	10.0%	9.6%	10.2%	6.9%	5.1%	5.6%	4.9%	4.1%	4.2%	3.9%	3.5%	1.5%	1.6%	1.5%	1.5%
20	8.7%	8.5%	8.5%	7.6%	5.2%	4.9%	4.8%	4.2%	3.2%	3.6%	3.3%	3.0%	1.3%	1.7%	1.4%	1.5%
25	6.5%	5.4%	6.7%	4.7%	4.0%	3.2%	3.1%	3.1%	2.7%	2.3%	2.0%	2.1%	1.2%	1.1%	1.0%	1.1%
30	5.3%	4.5%	4.5%	3.9%	2.4%	2.1%	2.0%	1.9%	1.0%	1.3%	1.2%	1.1%	0.7%	0.6%	0.5%	0.7%

Table 2: Experimental results for *RC* ladder with a source of variation with $\mu=0$, $\sigma=1$, and skew=0.5

Node	Elmore				D2M				TFA				Mixed (TFA+AWE)			
	Delay		Slew		Delay		Slew		Delay		Slew		Delay		Slew	
	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
10	14.5%	15.5%	15.1%	15.6%	9.3%	9.4%	9.3%	8.9%	7.3%	7.2%	7.9%	7.2%	2.4%	2.4%	2.3%	2.1%
15	14.1%	14.3%	14.2%	14.3%	7.9%	7.1%	7.6%	7.9%	6.1%	5.2%	5.9%	6.5%	1.6%	1.8%	1.8%	1.9%
20	12.3%	12.6%	12.3%	12.1%	6.2%	6.9%	5.8%	5.2%	5.2%	4.2%	4.2%	4.7%	1.5%	1.6%	1.6%	1.3%
25	7.4%	8.7%	7.9%	6.1%	3.8%	3.9%	4.1%	4.1%	3.3%	3.4%	3.2%	3.6%	1.4%	1.4%	1.5%	1.4%
30	5.5%	5.9%	6.3%	5.9%	3.6%	3.4%	2.5%	2.9%	2.2%	2.1%	2.7%	2.4%	1.2%	1.3%	1.2%	1.1%