A New Design for Double Edge Triggered Flip-flops*

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Abstract -- The logic construction of a double-edge-triggered (DET) flip-flop, which can receive input signal at two levels of the clock, is analyzed and a new circuit design of CMOS DET flip-flop is proposed. Simulation using SPICE and a 1 micron technology shows that this DET flip-flop has ideal logic functionality, a simpler structure, lower delay time and higher maximum data rate compared to other existing CMOS DET flip-flops. By simulating and comparing the proposed DET flip-flop with the traditional single-edge-triggered (SET) flip-flop, it is shown that the proposed DET flip-flop reduces power dissipation by half while keeping the same date rate.

I. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power considerations were mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed in VLSI design.[1] One of the primary driving factors has been the remarkable success and growth of the class of wireless communications systems (personal digital assistants and personal communicators) which demand high-speed and complex functionality with low power consumption.

In a digital system, synchronization/clocking has its special role. By its action as a timing signal the system clock controls the working rhythm of the chip. If the system is considered as a set of interconnected gates and flip-flops, the clock signal controls all flip-flops to sample and store their input data synchronously. Therefore, the clock signal tends to be highly loaded. In addition, to distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the capacitance of the clock net which also happens to have the largest activity (2 transitions per cycles) in a synchronous circuit (ignoring possible hazard activity on same signal lines). Recent studies indicate that the clock signals in digital computers consume a large (15% - 45%) percentage of the system power.[2] Thus, reducing power dissipation due to the clock net is an important task in LSI designs, such as the wireless communication system.

* This work was supported in part by DARPA under contract # F33615-95-C-1627 and Project No. 9713034 of CNPC

If we investigate the basic process that the clock signal controls a flip-flop, we will find that the efficiency of the clock is only 50%. Low and high levels of the clock signal put a latch in either a storage state or an input state. In the storage state, the clock level switches off the input path, and, the input data is thus rejected, while in the input state, the clock level allows the input signal to travel to the output terminal of the latch. However, if input date can be received and sampled at both levels of the clock, the flip-flop will receive and process two data values in one clock period. In other words, the clock frequency could be reduced by half while keeping the data rate the same. This means that under the requirement of preserving the original circuit function and data rate, the dynamic power dissipation due to clock transitions can be reduced by half. It is expected that the half-frequency reduced clock system is useful in low power systems (including wireless, battery operated systems).

How to sample and store the input data at both clock levels? We consider two related problems. The first problem is to restructure the flip-flop so as to sample and store the input data at both of its edges. This is precisely a double-edge-triggered (DET) flip-flop,[3-7] which samples the input data by both the clock's rising edge and falling edge. The second problem is to use the traditional single-edge-triggered (SET) flip-flop (for example, sensitive to clock's falling edge) to compose a new storage system, which can sample the input data on the clock's rising edge as well as its falling edge. As to the first challenge, this paper investigates the principles of the DET flip-flop design and presents a logic structure based on multiplexors (MUX), which is used to realize this type of flip-flop. Furthermore, a new circuit design of a CMOS DET flip-flop is described. By using computer simulation, the proposed design is compared with the traditional SET flip-flop. Results show that the DET flip-flop exhibits a 2x power saving factor. Besides, comparison of this DET flip-flop with ones reported by other researches show that our design has a simpler structure, less delay time and higher maximum data rate. As to the second challenge, this paper proposes a new double-edge-triggered storage device, which is composed of traditional SET flip-flop, but receives data at both edges of the clock. This design can also be used for reducing power dissipation while preserving the

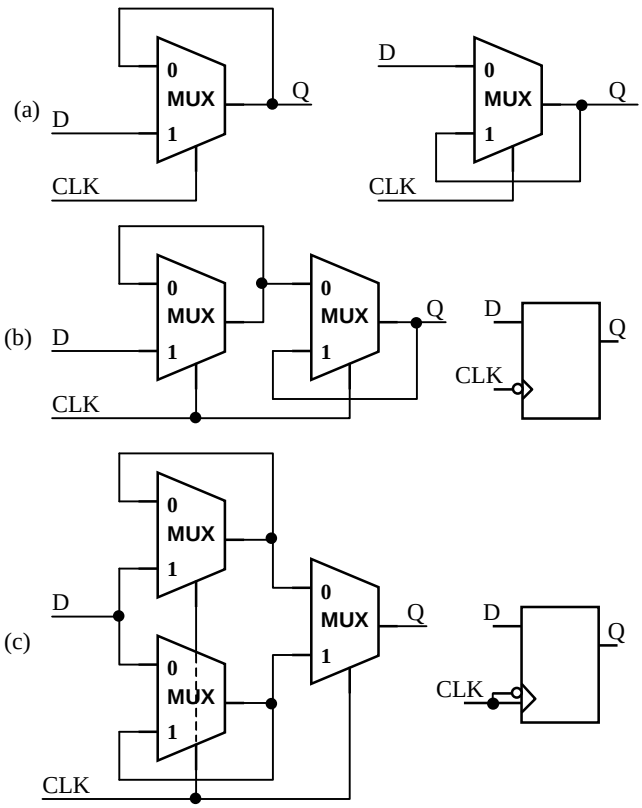


FIGURE 1 (a) Positive and negative level-sensitive latches; (b) SET flip-flop; (c) DET flip-flop

data throughput or doubles the data throughput while preserving the power dissipation.

II. LOGIC STRUCTURE OF A DET FLIP-FLOP

Latch is the basic unit for composing a flip-flop. The levels of a clock, *CLK*, are used to drive the latch to either the storage state or the input state. If we use *D*, *Q* and *Q'* to express the input signal, present state and next state of a latch, the state equations for positive and negative level-sensitive latch can be expressed as:

$$Q' = D \cdot CLK + Q \cdot \overline{CLK} \qquad (1)$$

$$Q' = D \cdot \overline{CLK} + Q \cdot CLK \qquad (2)$$

Equation (1) describes a latch which passes the input data when *CLK* = 1 and stores it when *CLK* = 0. Inversely, equation (2) describes a complementary latch, which receives input data at *CLK* = 0 and stores it at *CLK* = 1. The corresponding logic structures can be realized with a MUX, as shown in Fig.1(a).

If two complementary latches are connected in series, one will be in the storage state while other is in the input state and a "non-transparent" edge triggered flip-flop is formed. Taking the latches in Fig.1(a), they can compose a well known "master-slave flip-flop" as shown in Fig.1(b).[8] When *CLK* = 1, its master latch passes input data and its slave latch is in the storage state; when *CLK* = 0, its master latch will be in the storage state and its slave latch will pass and output the signal stored by the master latch. Therefore, this flip-flop changes its state at the clock's falling edge and keeps its state unchanged at the clock's rising edge.

The above discussion shows that the master latch does not receive the input data when *CLK* = 0. Obviously, if the input data has to be received at both clock levels, these two complementary latches should be connected in parallel rather than in series. Then we can obtain a "side-by-side flip-flop" as shown in Fig.1 (c). Since the flip-flop is required to be non transparent from input to output, the output terminal should always be connected to the latch which is in storage state. Therefore, the MUX framed by the dotted line is needed. Because the flip-flop's state can change at both falling and rising edges of the clock, it is named "Double-Edge-Triggered Flip-Flop" and is denoted by the legend shown in Fig.1 (c).

III. A NEW DESIGN OF CMOS DET FLIP-FLOP

The MUX can be realized with two CMOS transmission gates, therefore, the logic structure in Fig.1(c) can be easily used to design the CMOS DET flip-flop as shown in Fig.2(a).[7] Note that two inverters are inserted in the feedback path to restore the level in two latches. Besides, all three MUXs are simply composed of a pair of MOS transistors for reducing number of transistors.

We propose a new circuit design of CMOS DET flip-flop shown in Fig.2(c). It has the same number of transistors as a traditional CMOS SET flip-flop as given in [8]. At the same data rate we simulated both of these flip-flops using SPICE and a 1μ technology, while taking an inverter as the load. Their transient analysis waveforms are shown in Fig.3. Results confirm that the CMOS DET flip-flop can keep the same data rate while working at half the frequency which leads to a 2x reduction in power dissipation. We use the power meter[9] to measure and compare the power dissipation of two types of flip-flops for an input sequence 011000110001. Results show that the DET flip-flop can reduce power dissipation by half ($\approx 62\%$).

Reference [7] points out that a random sequence of *n* bit input causes $(n + 1)/2$ expected changes in each latch of the SET flip-flop, but only $(n/2 + 1)/2$ expected changes in each latch of the DET flip-flop. With our input sequence, there are five changes ($0 \to 1 \to 0 \to 1 \to 0 \to 1$) in each latch of both SET and DET flip-flops. This means that the chosen sequence is rather conservative in estimating the power reduction with DET flip-flop. A detailed comparison between two kinds of flip-flops is given in Table 1, which shows the

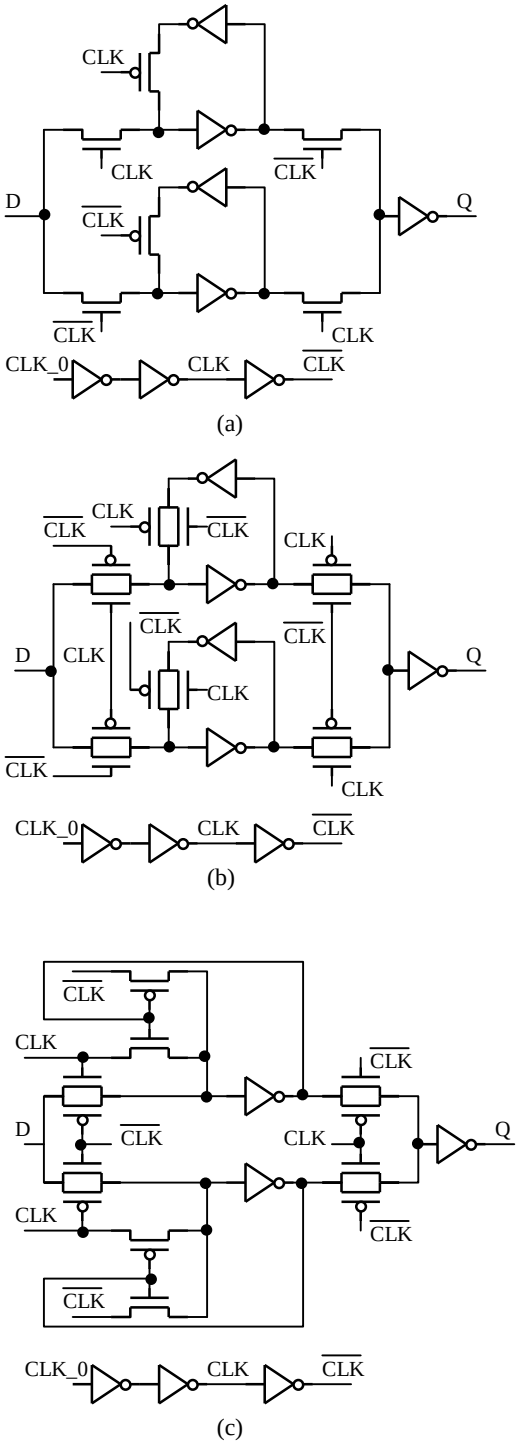


FIGURE 2 (a) The design of CMOS DET flip-flop in Ref.[7];
(b) A modified design of CMOS DET flip-flop;
(c) The new design of CMOS DET flip-flop.

higher quality of the DET flip-flop. In this table the delay time is defined as the clock-to-*Q* delay, that is the delay from the active clock input to the new value of the *Q* output.[8] Since the new value is stored in the master latch in the SET flip-flop and passed through the slave latch to the output after

TABLE 1 COMPARISON OF SET FLIP-FLOP AND DET FLIP-FLOP

	SET flip-flop	DET flip-flop
average delay time	0.72 ns	0.57 ns
maximum data rate	550 Mbits/s	900 Mbits/s

TABLE 2 REPORTED RESULTS OF VARIOUS STATIC CMOS DET FLIP-FLOPS

(data taken from relevant references)

design	number of transistors	maximum data rate	average delay time	power reduction
Ref. [4]	28	100 Mbits/s	3 ns	----
Ref. [6]	20	500 Mbits/s	----	----
Ref. [7]	18*	125 Mbits/s	----	21 %
Fig. 2(c)	20	900 Mbits/s	0.57 ns	62 %

TABLE 3 RESULTS WITH THE SAME SIMULATION CONDITION

design	number of transistors	maximum data rate	average delay time	power reduction
in Ref. [4]	28	500 Mbits/s	1.54 ns	22 %
in Ref. [7]	18	550 Mbits/s	0.61 ns	52 %
Fig. 2(c)	20	900 Mbits/s	0.57 ns	62 %
Fig. 2(b)	24	700 Mbits/s	0.63 ns	66 %

the triggering clock transition comes, the average delay time is a little bit longer than that of the DET flip-flop. If we feedback the output of the load inverter to the input of DET flip-flop, we can observe the maximum frequency of the flip-flop.[5,7] The maximum clock frequency for DET flip-flop is measured to be 450MHz, however, its maximum data rate should be doubled as shown in Table 1.

A comparison of the simulation result with ones reported in Refs.[4,6,7] are listed in Table 2. Which shows that our design has a simpler structure, lower delay time and higher maximum date rate. We should point out that the technology used in Refs. [4],[6],[7] are 2μ, 1.5μ, and 2μ, respectively. Besides, all MUXs used in Ref. [7] are simply composed of two pass transistors so it has the least transistor count.

For a fair comparison we use the same SPICE simulator and 1μ technology to simulate all presented circuits. Results are given in table 3, where the design in Ref.[6] has been omitted since it requires transistor sizing in the new technology which we wanted to avoid. Besides, we also simulated a modified DET flip-flop in Fig.2(b), which use transmission gates to replace all pass transistors in Fig.2(a). Under the same input sequence 011000110001 the energy dissipation (including both flip-flop itself and the buffers on the clock tree) diagrams in Fig.4 shows that a DET flip-flop consumes significantly lower power compared to a conventional SET flip-flop.

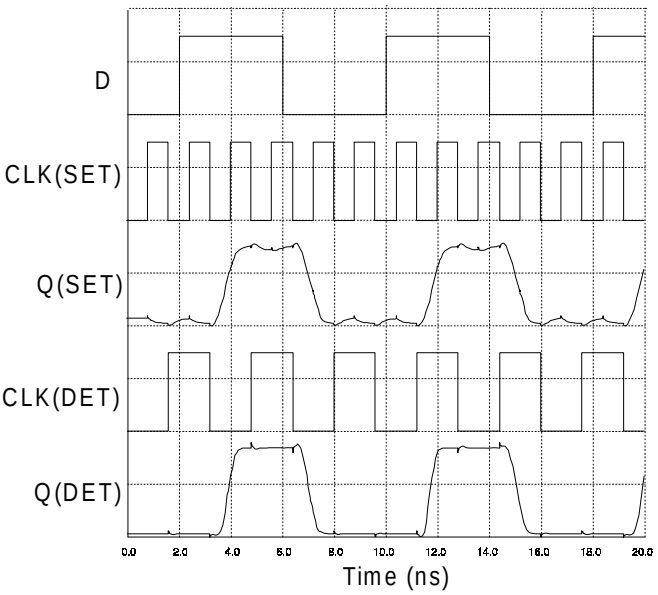


FIGURE 3 Transient analysis waveforms

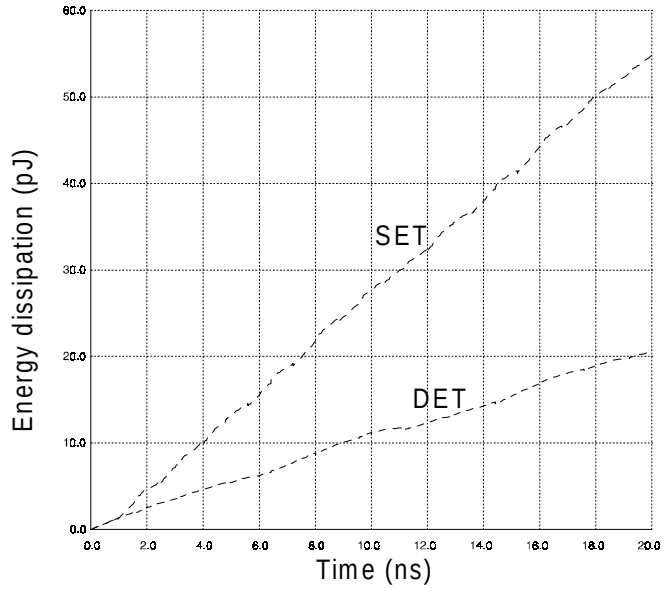
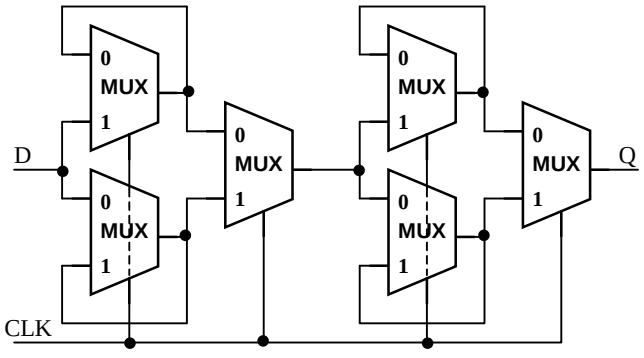
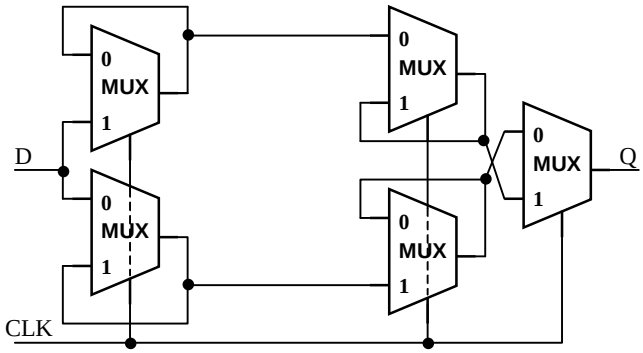


FIGURE 4 Energy dissipation diagram



(a)



(b)

FIGURE 5 (a) Connection of two DET flip-flops in series;
(b) Equivalent structure with SET flip-flops.

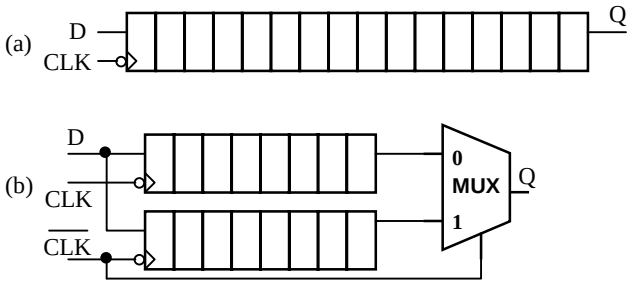


FIGURE 6. 2n-bit serial-in/serial-out shift register
(a) SET design;
(b) DET design using SET flip-flops.

IV. DET DEVICES BASED ON TRADITIONAL SET FLIP-FLOP

Dynamic DET flip-flops have been also investigated[5-6] based on the assumption that the DET flip-flops could be connected in series to form a shift register. Figure 5(a) shows two DET flip-flops connected in series, which form a 2-bit shift register. The resulting logic function is the same as the function of the logic structure shown in Fig.5(b). We notice that the latter structure is simply composed of two traditional SET flip-flops with opposite edge-triggering mechanisms connected in parallel and output switched by a MUX. This example hints that the traditional SET flip-flop can be also used to form a 2-bit register which is double-edge-triggered. The reason we can use two levels of the clock in Fig.1(c) is that the latches are arranged in parallel and receive the input data alternately. Thus, if these latches are replaced by traditional SET flip-flops with complementary clocks, the resulting structure is a "double-edge-triggered" 2-bit shift register. This is especially important when designing a 2n-bit serial-in/serial-out shift register as shown next.

Suppose 2n=16, a traditional shift register can be realized by using sixteen SET flip-flops cascaded in series, as shown in Fig.6 (a). Sixteen clock periods are needed for it to store or output a 16-bits data in series. During this time each one of the sixteen flip-flops receives 32 clock transitions. A dual-rail

structure, which can receive input date at two both levels of the clock, is shown in Fig.6 (b). The input data are received by the upper or the lower flip-flop in turn in one clock period. The input data are stored in turn and are switched in turn to the output. This time only eight clock periods are needed. During this time, each one of sixteen flip-flops receives only 16 clock transitions. Therefore, if we keep the clock frequency unchanged, then the throughput is doubled while maintaining the same power dissipation level. On the other hand, if we reduce the clock frequency by a factor of 2, the power dissipation goes down accordingly and the throughput remains the same.

V. CONCLUSION

This paper studied the techniques by which the storage elements in a VLSI system, such as the wireless system, can receive, sample and store the input data at the two levels of the clock to reduce the clock frequency and power dissipation in the related clock system. This paper discussed the logic structures of DET flip-flop based on MUX. A new design of CMOS DET flip-flop was proposed and simulated with SPICE and 1μ technology. The simulation results show:

(1) The proposed new circuit design of DET flip-flop has ideal logic function. It can receive, sample, and store the input data at the same data rate but at half the clock frequency in comparison with the traditional SET flip-flop. The circuit power is reduced when using the DET flip-flops.

(2) By analyzing the simulation results of designed CMOS DET flip-flop and the traditional CMOS SET flip-flop the former has not only lower delay time, but also higher maximum data rate since its latch in storage state is closer to the output.

(3) By comparing the simulation results of the designed CMOS DET flip-flop with ones reported in Refs.[4,6,7] it was found that our design has a simpler structure, less delay time and the highest maximum date rate. In addition, we simulated an improved DET flip-flop and found that this DET flip-flop has the most prefer low power quality.

This paper indicates that if the DET flip-flops are connected in series the structure can be simply replaced by two SET flip-flops connected in parallel. Based on it we propose a new double-edge-triggered storage design, which is composed of traditional single-edge-triggered flip-flop.

This work shows that if a half-frequency reduced clock system is adopted in VLSI design, the power dissipation of the clock tree and the DET storage elements will be reduced by half while keeping the data rate unchanged.

REFERENCES

[1] M. Pedram, "Power minimization in IC Design: Principles and applications," *ACM Transactions on Design Automation of Electronic Systems*, vol. 1, pp.3-56, Jan. 1996.

[2] G. E. Tellez, A. Farrah and M. Sarrafzadeh, "Activity-driven clock design for low power circuits," in *Proc. IEEE ICCAD*, San Jose, pp.62-65, Nov. 1995.

[3] S. H. Unger, "Double-edge-triggered flip-flops," *IEEE Trans. Computers*, vol.30, no.6, pp.447-451, June 1981.

[4] S. L. Lu and M. Ercegovac, "A novel CMOS implementation of double-edge-triggered flip-flops," *IEEE J. Solid-State Circuits*, vol.25, pp.1008-1010, Aug. 1990.

[5] M. Afghahi and J. Yuan, "Double edge-triggered D-flip-flops for high-speed circuits," *IEEE J. Solid-State Circuits*, vol.26, no.8, pp.1168-1170, Aug. 1991.

[6] A. Gago, R. Escano and J. A. Hidalgo, 'Reduced implementation of D-type DET flip-flops," *IEEE J. Solid-State Circuits*, vol.28, no.3, pp.400-402, Mar. 1993.

[7] R. Hossain, L. D. Wronski and A. Albicki, "Low power design using double edge triggered flip-flops," *IEEE Trans. VLSI Systems*, vol.2, no.2, pp.261-265, June 1994.

[8] N. H. E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A System Perspective*, 2nd ed. Reading MA: Addison-Wesley, 1993.

[9] S. M. Kang, "Accurate simulation of power dissipation in VLSI circuits," *IEEE J. Solid-State Circuits*, vol.21, no.5, pp.889-891, Oct. 1986.