Crosstalk-Affected Propagation Delay in Nanometer Technologies

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ABSTRACT

This paper presents a detailed analysis of the crosstalk-affected delay of coupled interconnects considering process variations. We utilize a distributed RC-π model of the interconnections to accurately model process variations. In particular, we perform a detailed investigation of various crosstalk scenarios and study the impact of different parameters on crosstalk delay. While accounting for the effect of correlations among parameters of the neighboring wire segments, statistical properties of the crosstalk-affected propagation delays are characterized and discussed. Monte Carlo-based simulations using Spice demonstrate the effectiveness of the proposed approach in accurately modeling the correlation-aware process variations and their impact on interconnect delay in the presence of crosstalk.

Keywords

Correlation, crosstalk-affected delay, process variations, statistical static timing analysis, skew, variation shielding

1. INTRODUCTION

The increase in package density as well as the clock frequency of the VLSI circuits has made noise, such as the capacitive coupling noise, one of the most challenging problems in the design and verification of modern VLSI circuits. Furthermore, the interconnect lines get thicker and narrower (and longer in case of global interconnects), which all result in the aggravation of crosstalk noise amplitude and duration, and the circuit faults caused by such noise sources. Therefore as the VLSI technology scales down the role of interconnect parasitic effects in the signal integrity becomes increasingly more pronounced.

Another unwanted side effect of CMOS process technology scaling is the increase in process variations. Differences between identical features in a certain lithographic process are referred to as process variations. Lithography steps generate more process variations in smaller geometric feature sizes. Therefore, cell and interconnect delay characterization methods should consider the increasing impact of process variations on circuit performance and reliability. In addition to IC manufacturing process variations, environmental variations, and device/interconnect aging processes create a rather large deviation of key circuit parameters from their designed values. These phenomena in turn produce timing uncertainty and demand highly sophisticated and robust crosstalk-aware analysis and optimization tools.

The conventional corner-based techniques, to handle variability of parameters will not be effective in nanometer technologies due to their highly pessimistic (and sometimes optimistic) views. Statistical analysis is viewed as an essential methodology for nanometer process technologies, which enables application of the actual statistics of the process technology parameters for the accurate calculation of design characteristics such as delay and noise [1].

Crosstalk effect has been analyzed using lumped RC models to find simple close-form formulas for crosstalk-induced pulse and slowdown in [2]-[5]. However, this model is inaccurate for global interconnects, especially at high clock frequencies. Using a distributed coupling capacitance model produces more accurate and realistic results. Closed-form expressions by using 2π and 4π configurations (which are based on linear circuit models) have been developed in [6] and [7], respectively. However, the quality of analysis and optimization tools degrades when using linear equations to model the nonlinear behavior of drivers. In [8] and [9] distributed RC modeling has been used to estimate the pulse induced by crosstalk effect. In [10], by using distributed RC model with a circuit simulation engine, a number of interesting observations have been reported for weak spot defects in the presence of crosstalk noise. Indeed, deriving accurate closed-form expressions based on distributed RC modeling has been a difficult, and so far unsatisfactory, undertaking. As a result, it is common practice to make simplifying, yet realistic, assumptions about the crosstalk noise in order to mitigate the complexity of crosstalk-affected analysis and optimization.

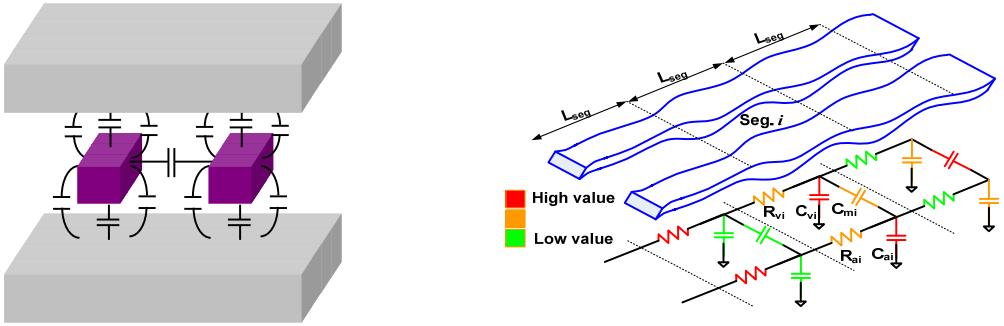
Although a great deal of research has been done on statistical static timing analysis, only a few approaches exists in literature that investigate the impact of process variations on crosstalk and inherently circuit performance. The statistical model of [11] uses a lumped RC model to explore crosstalk-induced pulse (glitch) effect, where a single resistance is

extracted to capture the effect of total self resistance of interconnect, regardless of its length. The case for self and coupling capacitances is similar. Also the correlation between the circuit parameters, such as interconnect line resistance and capacitance is assumed to be zero. The statistical model proposed in [12] is more sophisticated and uses a circuit model with higher number of nodes; however, still a single capacitance is extracted to model the total coupling effect, which makes it inappropriate for long interconnect lines. The authors of [13] apply special exponential waveform shapes to analytically study the statistics of crosstalk effect. However the exponential type waveforms cannot accurately represent noise-affected signal waveforms. Additionally, the above approaches are unable to consider the correlation between neighboring wire segments.

The goal of this paper is to study the effect of process variations on some existing crosstalk analysis techniques, resolve their shortcomings, and finally propose an efficient model to statistically calculate the crosstalk-affected delay of the interconnect victim line. More precisely, first a distributed RC-π model is used to accurately capture the statistical variations in the physical dimensions of the interconnect lines and the corresponding electrical parameters. We first provide the results of our extensive simulation of crosstalk-affected delay and a number of important properties of the crosstalk that may be exploited in validation and optimization tools to increase the accuracy of crosstalk effect analysis and reduce the computational complexity of these tools. In addition, we study the sensitivity of the delay and transition time of the output a crosstalk site to circuit parameters such as its coupling, wire capacitance, and resistance values, and the driver strength, as well as the timing parameters, namely the input skew and the input transition time. The local effects of process variations on the coupled wire segments and the correlations among variations in neighboring segments are considered in statistical analyses. This information is then used to evaluate the correctness of the existing crosstalk analysis techniques in the presence of process variations using extensive sets of Monte Carlo simulations to calculate the actual statistical distribution of victim line timing parameters. Finally based on our observations, we propose a set of heuristic solutions for each technique to improve their applicability in statistical analysis of crosstalk effects. The paper is a major extension of our conference papers [14] and [15].

Capacitive coupling between a pair of interconnect lines can induce spurious pulses and/or cause delay effects. We refer to such effects as crosstalk-induced effects. The portion of the layout where the coupling occurs is referred to as a crosstalk site. Crosstalk-induced slowdown occurs when an aggressor line, A, and a victim line, V, make signal transitions (state changes) in opposite directions. The net effect, in theory, of the coupling between the two lines is that the transition on the aggressor line tends to slow-down the transition on the victim line, making it appear to be delayed in time. The amount of slow-down is the difference between the time the signal transition at the far-end of the victim line crosses $0.5V_{dd}$ when the aggressor has made a transition in the opposite direction, and that when the aggressor remains quiet. Slowdown is dependent on the victim and aggressor signal transition times, the skew between their signal arrival times, and the parameter values that are reflected in the capacitive and resistive model components. The uncertainty about the crosstalk-induced delay increase/decrease may be due to variations in any of the above parameters.

Consider a pair of coupled interconnect lines in some metal layer, which lies in between two dielectric plates (cf. Figure 1(a) in which one segment of the coupled interconnect is depicted.) The two interconnect lines run in parallel and are capacitively coupled. Either line can be considered as a victim, while the other may be treated as the aggressor. The goal is to statistically analyze the slowdown of the victim line due to aggressor line activity. A distributed RC-π model (cf. Figure 1(b)) is used to accurately model the abovementioned interconnect line configuration. In this circuit, each RC-π stage represents an interconnect segment of a predefined length, L_{seg}, which is an important factor when considering spatial correlation among physical. The coupling between two interconnect lines along segment i is captured by the coupling capacitance C_{mi}. The self capacitance and resistance of the victim interconnect in segment i are denoted by C_{vi} and R_{vi}, respectively. Note that although lengths of all wire segments are identical, due to process variations, parameter values for each segment are different from those for other segments.



(a) (b)

Figure 1: Distributed capacitive modeling of coupled interconnects.

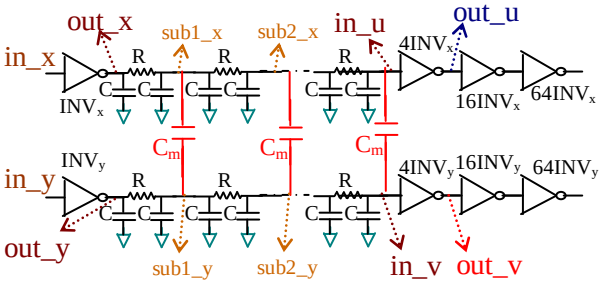
The complexity of distributed RC-π circuit model significantly limits its application in real world designs where millions of interconnect lines and hence crosstalk sites are present. Therefore, circuit designers try to derive the electrical behavior of this complex circuit model by approximating its transfer function using different model order reduction techniques [16]. Generally speaking, the existing models for coupled interconnects tend to be inaccurate when significant process variations exist. On the other hand, the complexity of model order reduction techniques significantly increases when considering process variations [17].

The remainder of this paper is organized as follows. Sections 2 to 4 focus on the slowdown effect of the crosstalk. Section 5 deals with crosstalk speedup effect. In sections 6 to 8 we study the driver strength, side load, and the interaction of crosstalk sites. In section 9 the basic aspects of interconnect characterization and modeling considering process variations, their local effects and correlation between parameters are reviewed. Section 10 explains the experimental setup used for simulation of coupled interconnects in the presence of process variations. Sections 11 summarize the conclusions.

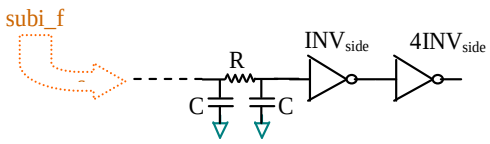
2. CROSSTALK SENSITIVY ANALYSIS: DEPENDENCE ON INPUT SKEW

Timing analysis is an essential aspect of determining whether a crosstalk event can create a faulty output in a circuit. In particular, the signal arrival times and transition times (inverse of slew rates) in a circuit can change as a function of the crosstalk noise that is present in the circuit. Therefore, the accuracy of timing analysis tools strongly depends on the accuracy of arrival time and transition time calculations in the presence of crosstalk noise. In this paper, we adopt the standard definition of arrival time and transition time that is commonly used in static and statistical timing analysis and ATPG tools, meaning that the *arrival time* of a signal transition is set to the time instance at which signal waveform crosses the $0.5V_{dd}$ voltage level whereas the *transition time* of a signal transition is defined as the slope of a line connecting two specific points on the noisy input: the points are when the signal waveform crosses the $0.1V_{dd}$ and $0.9V_{dd}$ voltage levels. The *skew* between two signal transitions is the difference between their arrival times. In this paper, we adopt the standard definition of arrival time and transition time that is commonly used in timing tools, meaning that the *arrival time* of a signal transition is set to the time instance at which signal waveform crosses the $0.5V_{dd}$ voltage level whereas the *transition time* of a signal transition is defined as the slope of a line connecting two specific points on the noisy input: the points are when the signal waveform crosses the $0.1V_{dd}$ and $0.9V_{dd}$ voltage levels. The *skew* between two signal transitions is the difference between their arrival times.

All experiments in this section through section 8 use configurations that are similar to the one depicted in Figure 2(a). In this configuration, the inverter $4INV_x$ is fed by a long interconnect line which is a potential crosstalk victim (The size of $eINV_f$ is *e* times as big as that of INV_f, where *e* can be 1, 4, 16, and 64 and *f* can be *x* and *y*.) Aggressor and victim lines run parallel to one another. Every 100µm long and 0.200µm wide wire segment is modeled by a single stage of an RC-π structure. For example, for a 1000µm wire pair we use 10 RC-π stages as depicted in Figure 2. The coupling of each stage is modeled by C_m; clearly, for a 1000µm wire pair the total coupling value is 10 times the C_m value. We perform our circuit simulations with the TSMC 0.13µm technology and use standard cells from a 130nm, 1.2V production cell library. The sheet resistance of metal interconnect in this technology is 0.074000Ω/square. The unit line capacitance is 22.6pF/meters. Therefore for a 1000µm wire, the total line resistance is 370Ω and the total self capacitance (capacitance to the ground) of each line is 22.6fF. From now on, we will refer to INV_x and INV_y as the *line drivers*. Similarly, $4INV_x$ and $4INV_y$ will be called the *line receivers*. We will refer to out_x and out_y (in_u and in_v) as the near-end (far-end) of the lines. Either line can be considered as a victim when the other is an aggressor. Figure 2(b) shows the side-load, which is used in some of our experiments.



(a) The crosstalk model for long parallel lines



(b) f ≡ x or y, sub0_x ≡ out_x, and sub0_y ≡ out_y

Figure 2: (a) The configuration used in our experiments, (b): The load configuration used in some of the experiments as the side-load, connected to the intermediate point i of line f.

We define the (normalized) *sensitivity* of variable p to variable q as $\sigma=(q.\Delta p)/(p.\Delta q)$. We say p is *insensitive* to q, when $\sigma\cong 0$; furthermore, p is *weakly sensitive* to q exactly if $0<\sigma<0.1$, and is *moderately sensitive* if $0.1<\sigma<1$; otherwise we say that p is *highly sensitive* to q. At times we will refer to Δp as *slowdown* or *speedup* of p depending on whether Δp is positive or negative, respectively. We will also use the term *crosstalk-affected delay and transition time* of node p to refer to the delay and transition time of that node when the impact of crosstalk capacitances are considered.

The sensitivity of crosstalk-induced slowdown to timing parameters, namely input skew and input transition times is studied in this section. It is shown that crosstalk-induced delay is highly sensitive to the input skew and weakly sensitive to the input transition time. Sensitivity analysis is useful for better understanding of the impact of the crosstalk noise on circuit performance. Considering the increase in process variations in current process technologies, the results of the sensitivity analysis may be used to create more accurate statistical models based on the variability of input parameters. As stated earlier, the accuracy of noisy signal arrival time and transition time calculation is crucial in timing analysis; therefore we report the dependence of delay as well as the transition time of the output (out_u and out_v) on the crosstalk noise.

2.1 Output Slowdown as a function of Input Skew

To study the sensitivity of the crosstalk-affected output delay to input skew, the coupled lines, x and y (shown in Figure 2,) have been considered. They run in parallel and each of them is 1000µm long. We create signal transitions with opposite directions at the inputs of line drivers, namely in_x and in_y, hence the signal transitions of both lines will be slowed down. The arrival time of a falling transition at in_y is set to 1000ps and the arrival time of a rising transition at in_x is swept from -1000 to +1000 ps; therefore the input skew between in_x and in_y changes from -1000ps to +1000ps. We also set their transition times to 100ps. Both out_u and out_v exhibit a crosstalk-induced slowdown in this case. Figure 3 shows the slowdown of out_u (delay of out_u w.r.t. in_x) and out_v (delay of out_v w.r.t. in_y.) Coupling capacitance is 300fF (C_m=30fF.) Inverter cells with nearly equal fall and rise time ratio is used for all INV cells in the configuration. We refer to such cells as balanced cells in this paper. Since the cells in this experiment are balanced cells the maximum slowdown at out_u and out_v are very close, e.g., they are less than around 75ps different in case of coupling capacitance of 300fF.

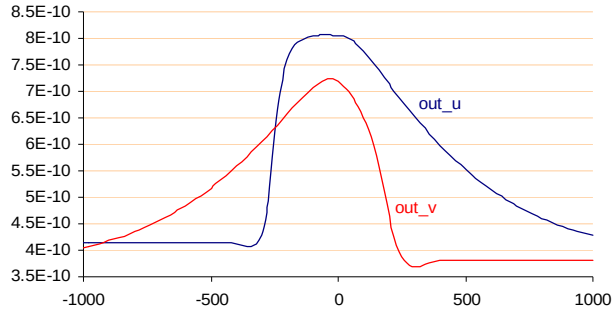


Figure 3: Delay from in_x (in_y) to out_u (out_v) as a function of input skew between in_x and in_y.

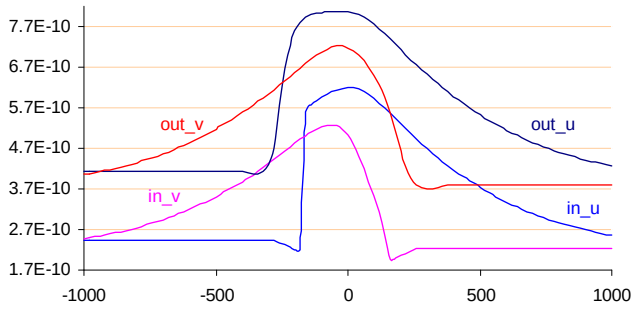


Figure 4: Delay from in_x (in_y) to in_u (in_v) and from in_x (in_y) to out_u (out_v) as a function of input skew.

P1: Crosstalk-affected delay can be highly sensitive to the input skew. Especially, for skew values that are close to the one generating the worst-case delay, a small change in the skew can significantly change the delay.

For example in Figure 3, a 25ps input skew change can result in more than 105ps of the delay change for out_u. P1 highlights the importance of accurately computing the signal arrival time in the presence of crosstalk noise.

P2: The worst-case crosstalk slowdown at the output of the victim line receiver occurs at a certain skew, but a significant slowdown (e.g., more than 20% delay increase) occurs with a large range of skews.

Our experiments confirm that even a zero-skew between transitions at the near-end of the lines, i.e., out_x and out_y, may not necessarily create the worst-case crosstalk-induced slowdown. Note that the crosstalk coupling of the aggressor and victim lines is distributed along the length of the lines and the crosstalk effect at one point of the victim line propagates and affects the subsequent points along the victim line. Therefore, the crosstalk effect at each point of the victim line is the summation of coupling effects of that point plus the delayed effects propagated from the preceding points. As a result, the maximum crosstalk slowdown occurs over a much wider window of time than is usually assumed. One way to reduce the crosstalk effect of a site is to deliberately change the delay of circuit lines driving the corresponding victim and/aggressor lines (e.g. by using buffers.) This can change the input skew such that the slowdown created by that crosstalk site cannot create any error. P2 shows that in order to significantly reduce the slowdown from its worst-case level, the input skew may have to be changed by a rather large amount.

P3: The maximum crosstalk slowdown does not necessarily occur for zero input skew condition even for completely symmetric interconnects.

P3 provides motivation for establishing a framework for alignment of multiple aggressors and the victim line such that the worst-case crosstalk effect is generated.

2.1.1. Slowdown effect at the far-end of the victim line.

In Figure 4 we report the slowdown of in_u (in_v) w.r.t. in_x (in_y) and compare this slowdown with results of Figure 3 (slowdown of out_u (out_v) w.r.t. in_x (in_y).

P4: Delay at the output of the victim line receiver, out_u (out_v), follows the shape of the delay at the far-end of the victim line, in_u (in_v).

2.2 Output Transition Time as a function of Input Skew

A new experiment similar to the one described in Section 2.1 is set up. The only difference is that now the transition time change at the interconnect output (out_u/out_v) due to the crosstalk effect is simulated. Figure 5 shows the dependence of transition time of out_u and out_v on the input skew. The following summarizes the observations made from this experiment.

P5: The output transition time can be highly sensitive to the input skew. Especially, for skew values that are close to the one generating the worst-case increase in transition time, a small change in the skew can significantly change the transition time.

For example in Figure 5 less than 20ps change in skew can result in more than 200ps increase in the transition time of out_u.

P6: The maximum transition time at the output of the victim line occurs for a certain input skew, with a significant increase in transition time occurring for a large range of input skew values.

P7: The maximum transition time at the output of the victim line receiver does not occur for the zero input skew even for completely symmetric interconnects. Moreover, the skew that results in the maximum transition time may not be the one that results in the maximum slowdown.

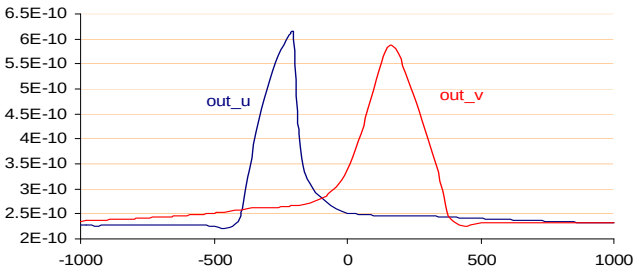


Figure 5: Transition times of out_u and out_v as a function of input skew.

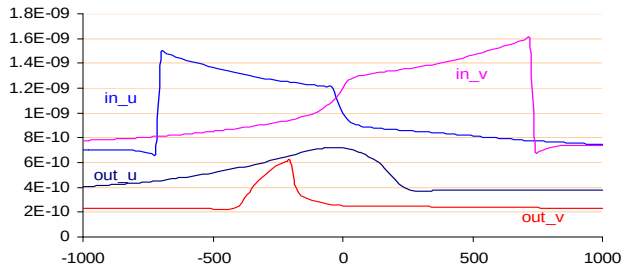


Figure 6: Transition times of in_u (in_v) and out_u (out_v) as a function of input skew.

2.2.1. Transition time change at the far-end of the victim line

In Figure 6 we compare the transition time of the signal transitions at the far-end of the victim line, i.e., in_u (in_v) with that of the output of the victim line receiver, i.e., out_u (out_v). In contrast to what we observed in Figure 4 for slowdown, the transition time comparison shows different characteristics.

P8: Electrical waveforms for the transitions at the far-end and the output of the victim line receiver differ significantly in terms of their characteristics.

In general the transition at the input of a gate tends to be smoothed out, and hence, the transition at the gate's output will not change as drastically as the change in the gate's input transition.

3. CROSSTALK SENSITIVITY: DEPENDENCE ON TRANSITION TIME

To study the effect of transition time of signals at the input of the victim line driver and/or the aggressor line driver, we keep the skew between the transitions at in_x and in_y fixed at zero. We apply a falling transition at in_y and a rising transition at in_x with identical arrival times so that both out_u and out_v will experience crosstalk-induced slowdown. We consider a reasonable range of transition times from 0 to 600ps.

We will consider two scenarios for the transition time change. In the first scenario, the transition times of both in_x and in_y are changed. In the second scenario, only one of the input transition times is changed while the other one is kept constant. A balanced inverter cell has been used for both INV cells in the configuration of Figure 2.

3.1 Both Input Transition Times Change

The transition time of in_x and in_y are identical and vary in lockstep from 0 to 600ps. Figure 7 illustrates how the slowdown of the transitions at out_u and out_v change based on change of transition times of in_x and in_y. It is seen that a 600ps increase in input transition time of both in_x and in_y causes only a 145ps slowdown for out_u (with a coupling capacitance value of 300fF.) Therefore, assuming equal transition times for the aggressor and victim inputs, the slowdown at the output of the victim line receiver is only weakly sensitive to its input transition time.

Comparing P12 with P1, we conclude that crosstalk-affected delay sensitivity to the input transition time is much lower than that to the input skew. This has the implication that, as far as crosstalk is concerned, the accuracy of arrival time computation is more important than the accuracy of transition time computation. Figure 8 illustrates how the transition time of the transition at the output of the crosstalk site, i.e. out_u/out_v would change when transition times of both in_x and in_y change. From this figure, a 600ps increase in the input transition time of both in_x and in_y changes the transition time at out_v by only 10ps.

3.2 Only One Transition Time Changes

We simulate the crosstalk effect by keeping transition time of the signal transition at in_y constant at 100ps and then changing transition time of in_x from 0 to 600ps. Other parameters have been set similar to those of the experiment reported in Section 3.1. Figure 9 shows the effect of transition time change at one input (in_x) on the slowdown seen at the outputs.

Considering in_y and out_v as the input and output of the victim line, there will be less slowdown at out_v if the transition time at the input of the aggressor line driver, in_x, increases.

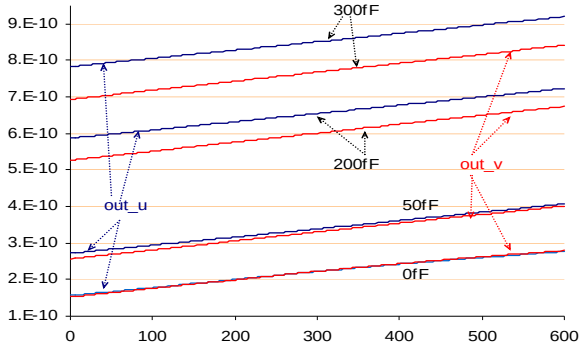


Figure 7: Delay from in_x (in_y) to out_u (out_v) as a function of input transition time (both transition times change) for different coupling capacitance values.

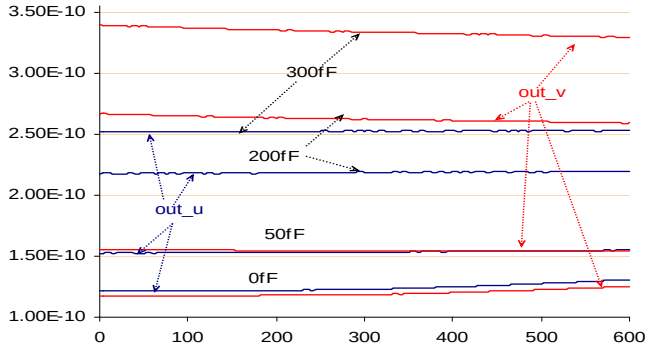


Figure 8: Transition times of out_u and out_v as a function of input transition time (both change) for different coupling values.

P9: Crosstalk-affected delay and transition time of the output of the victim line are only weakly sensitive to its input transition time.

P10: For a given transition time at input of the victim line driver, faster aggressor causes larger worst-case slowdown.

P11: The maximum slowdown occurs when the victim has the largest transition time whereas the aggressor has the smallest transition time.

Table 1 lists the slowdown for several interesting transition times taken from Figure 7 and Figure 9. In the last row, the slowdown values for the last three columns (664, 718, and 720) substantiate P14. Comparing the second column entry (920) with entries of columns 1, 3 and 4 (919, 805, and 785) substantiates P15. In Figure 10 we study a similar effect to what was presented in Figure 8. However, only transition time at in_x is changed.

P12: Slower aggressor creates slower transitions at the output of the victim line receiver.

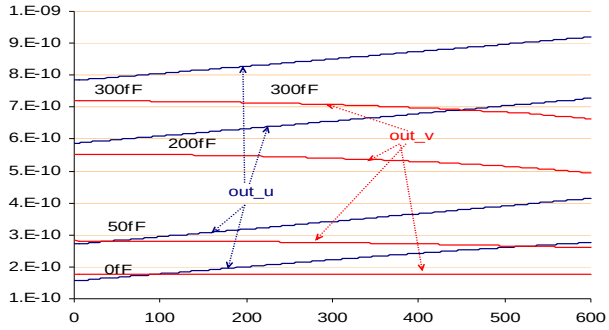


Figure 9: Delay from in_x (in_y) to out_u (out_v) as a function of transition time of in_x for different coupling values.

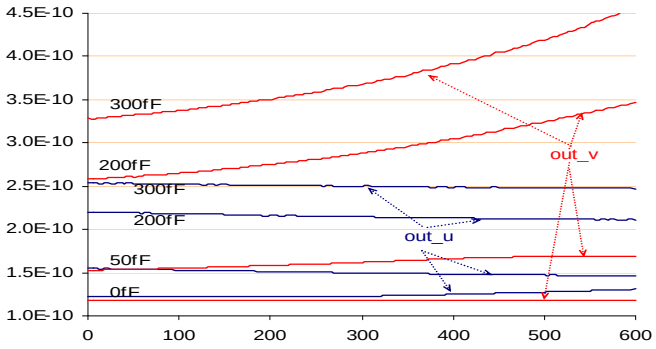


Figure 10: Transition time out_u (out_v) as a function of transition time of in_x.

4. CROSSTALK SENSITIVITY: DEPENDENCE ON CIRCUIT PARAMETERS

In this section we investigate the dependence of crosstalk-induced slowdown on the coupling capacitance value, wire capacitance, and wire resistance.

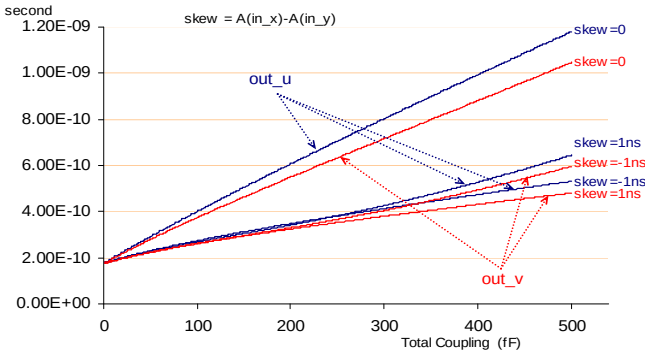


Figure 11: Delay from in_x (in_y) to out_u (out_v) as a function of coupling value for three different input skews.

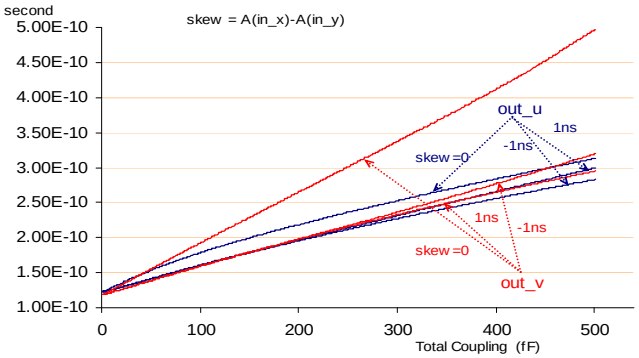


Figure 12: Transition times of out_u and out_v as a function of coupling value for different input skews.

4.1 Dependence on the Coupling Capacitance Value

The coupling (capacitance) value is the main factor in determining the magnitude of any crosstalk noise. Noise sensitivity analysis with respect to the coupling value are thus important to optimization algorithms such as wire spacing and buffer insertion, which aim at reducing the coupling value and subsequent minimization of the crosstalk effect. We ran the experiment described in Section 2.1 with different values of the coupling capacitance. The coupling capacitance value, C_m, was swept from 0 to 50fF, i.e., the total coupling between lines x and y was changed from zero to 500fF. The input skew was changed from -1ns to +1ns. However, for the sake of readability of the plots, only the results for three input skew values (i.e., -1ns, zero-skew, and +1ns) are provided. Figure 11 shows the slowdown of the output, out_u (delay of out_u w.r.t. in_x) and out_v (delay of out_v w.r.t. in_y.) Figure 12 provides the corresponding transition times.

As expected the crosstalk-affected delay is highly sensitive to the coupling value. Both output delay and output transition time are well approximated by a linear model. An important implication is that statistical analysis of crosstalk effect as a function of variability in C_m can accurately be modeled by a first order canonical model [18], i.e., there is no need for more complicated models such as the quadratic ones suggested in [19].

P13: Both slowdown and transition time increase at the output of the victim line receiver are highly sensitive to the coupling capacitance value. Furthermore, both of these quantities are well approximated by assuming a linear dependence on the coupling value.

Now we provide results for the same experiments as above but this time with respect to the input skew. For the sake of improved readability, results for only four coupling values are provided. Figure 13 shows the slowdown at the outputs, out_u and out_v, whereas Figure 14 shows the corresponding data of the transition time increase.

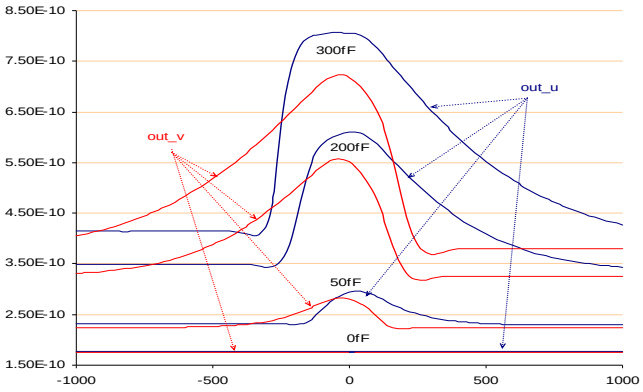


Figure 13: Delay from in_x (in_y) to out_u (out_v) as a function of input skew between in_x and in_y for different coupling values.

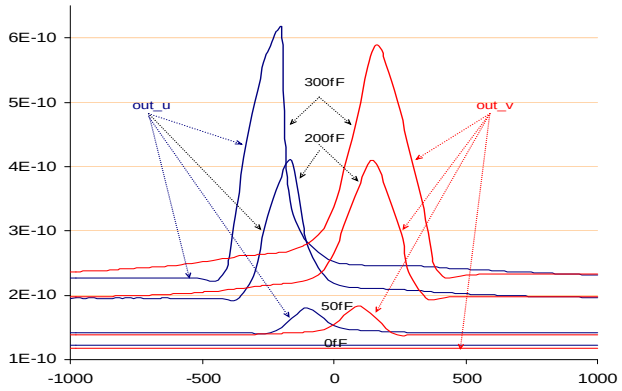


Figure 14: The transition times of out_u and out_v as a function of input skew for different coupling values.

P14: The input skew values that cause the maximum slowdown and largest transition time at the output of the victim line receiver are a strong function of the coupling capacitance value. However, increase in the coupling value, and hence crosstalk slowdown, does not necessarily result in an increase in the transition time.

Referring to Figure 14 and focusing on the skew range of about -200 to -100ps, we observe that the transition time of out_u for the case of 300f coupling is lower than that for 200fF, which confirms the latter part of observation P14.

It is worthwhile to mention that although throughout this paper we report the results of experiments performed on 1000µm parallel lines, we have confirmed that the results are equally valid for shorter lines. As an example Figure 15 shows the crosstalk-affected delay of the outputs versus the input skew for two lines which are 300µm each and run in parallel to one another (modeled by three stages of the RC-π structure.) It is seen that the results follow similar patterns to those for the 1000µm-long parallel lines.

transition time(in_x)	600	600	100	0
transition time(in_y)	600	100	100	100
delay(out_u)	919	920	805	785
delay(out_v)	841	664	718	720

Table 1: Crosstalk-affected delay sensitivity to the input transition time (in ps.)

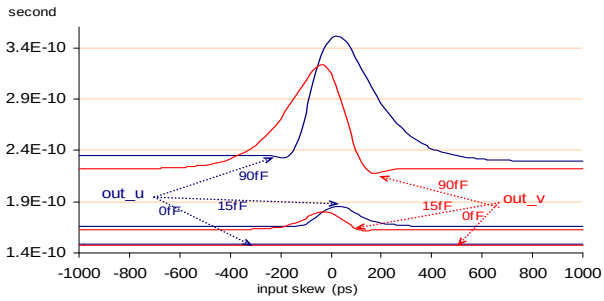


Figure 15: Delay from in_x (in_y) to out_u (out_v) as a function of input skew for two 300µm-long parallel lines.

4.2 Dependence on the Wire Capacitance

We performed a similar set of experiments to the ones in Section 2.1 in order to assess the sensitivity of crosstalk-induced output delay and transition time to the (self) wire capacitance value. The total wire capacitance for both wires is swept from zero to 500fF. Other parameters have been set as explained in Section 2.1. Figure 16 and Figure 17 show the output delay and transition time vs. the wire capacitance value, respectively. As before for readability purposes, the curves for only one coupling (300fF) and three input skew (-1ns, 0, +1ns) values are shown. Results for other coupling and input skew values are similar. As expected both the output delay and transition time exhibit a linear relationship with the wire capacitance.

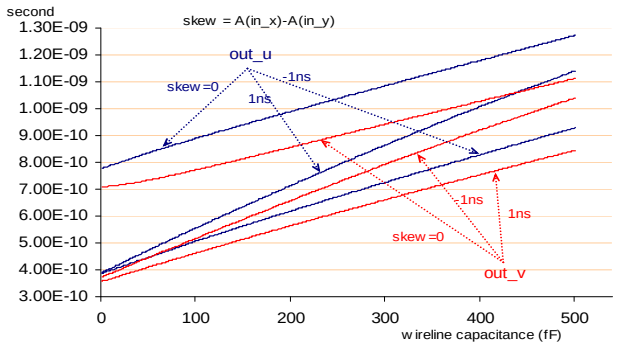


Figure 16: Delay from in_x (in_y) to out_u (out_v) as a function of the wire capacitance for three different input skew values.

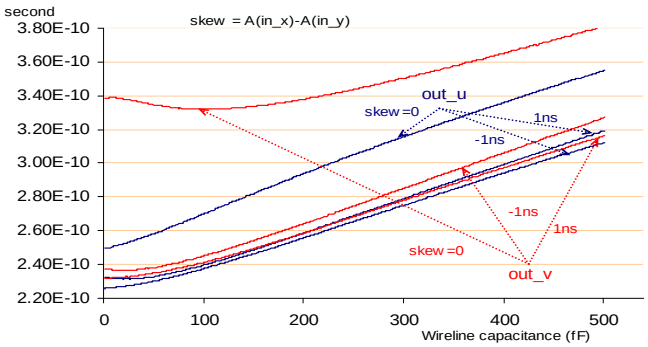


Figure 17: Transition times of out_u and out_v as a function of the wire capacitance for different input skew values.

To evaluate the crosstalk effect when the wire capacitance of only one of the coupled lines varies, we swept the wire capacitance of line x from zero to 500fF while keeping that of line y at a constant value of 22.6fF. Results are provided in Figure 18 and Figure 19.

Based on a lumped RC model for crosstalk noise analysis of [3] and [4] the crosstalk noise is inversely proportional to the wire capacitances of both the aggressor line and the victim line. However, our experiments show that this is not true. For example, in Figure 18, as the wire capacitance of line x increases the delay of that line also increases, i.e., the crosstalk-induced delay increases monotonically with the victim line wire capacitance. However, the delay of line y decreases for zero skew but increases for large skew values. This highlights the fact that the inverse proportionality relationship of the crosstalk-induced effect to the aggressor line wire capacitance is in general not valid. Similar behavior is seen in Figure 19 for the output transition time.

P15: The crosstalk-affected propagation delay is moderately sensitive to the wire capacitance value. In addition, it monotonically increases as the victim wire capacitance increases (victim output: out_u); However, it does not show a monotone behavior with respect to the aggressor wire capacitance (victim output: out_v.)

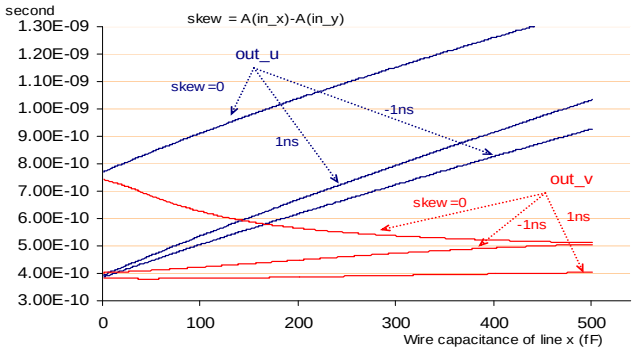


Figure 18: Delay from in_x (in_y) to out_u (out_v) as a function of wire capacitance of line x for three different input skew values.

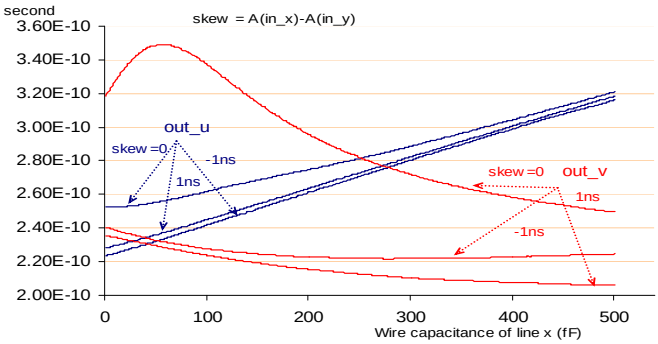


Figure 19: Transition times of out_u and out_v as a function of wire capacitance of line x for different input skew values.

In Figure 19, even the output transition time of out_u shows a non-monotone relationship with respect to victim line capacitance, i.e., the monotone behavior assumption of crosstalk-affected output transition time with respect to the wire capacitance of the victim or the aggressor line is in general invalid.

P16: The crosstalk-affected output transition time is moderately sensitive to the wire capacitance value, however in general it does not exhibit a monotone relationship with respect to victim or aggressor wire capacitance.

The corner-based worst-case analysis used in conventional STA or ATPG tools is generally assumed to be pessimistic. However, the above results show that it can also be optimistic. Due to lack of the monotone behavior property and the misconception about inverse proportionality of the crosstalk effect on the wire capacitances, the corner-based analysis can indeed underestimate the magnitude and severity of the crosstalk problem. For example, from Figure 18 the lack of the monotonic behavior for the slowdown w.r.t. the wire capacitance produces around 20ps delay underestimation at out_v for wire capacitance of 50fF (50% error considering the offset delay of 40ps for delay of out_v w.r.t. in_y.)

4.3 Dependence on the Wire Resistance

We swept the wire resistance of both lines from zero to 500 ohms and ran a similar set of experiments to the one described in Section 2.1. Figure 20 and Figure 21 show the results for a total coupling value of 300fF. The delay of both outputs monotonically increases; however, the output transition time may exhibit non-monotone behavior in some cases (cf. out_v transition time at zero skew in Figure 21.)

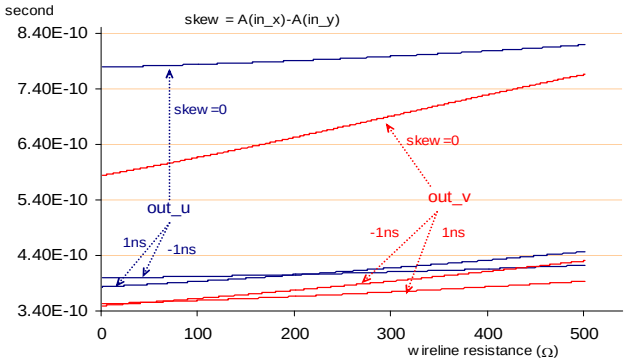


Figure 20: Delay from in_x (in_y) to out_u (out_v) as a function of the wire resistance for three different input skew values.

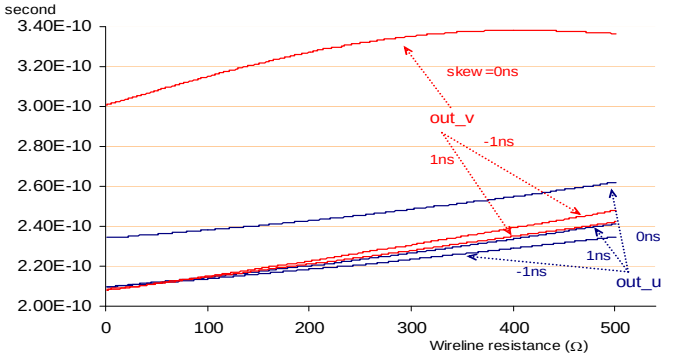


Figure 21: Transition times of out_u and out_v as a function of the wire resistance for different input skew values.

Figure 22 and Figure 23 contain the data for the case when the wire resistance of only line x is changed while keeping that of line y at a constant value of 370Ω. From Figure 22 the crosstalk-affected delay of the victim output (out_v) decreases when the wire resistance of the aggressor line (line x) increases. Also the delay of out_u increases which shows that the delay of the victim line increases with the increase in the victim line wire resistance. It is seen that both crosstalk-affected delay and transition time of the outputs can well be approximated by using linear equations.

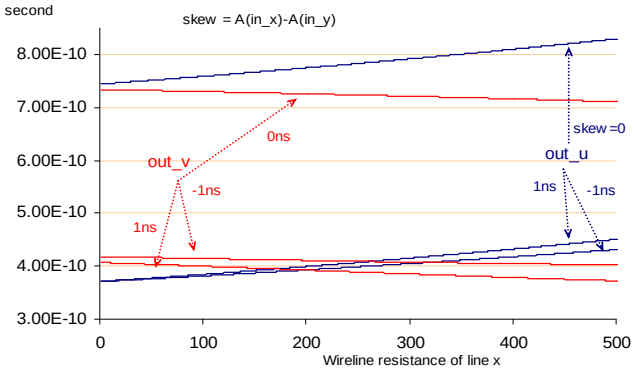


Figure 22: Delay from in_x (in_y) to out_u (out_v) as a function of the wire resistance of line x for 3 different input skew values.

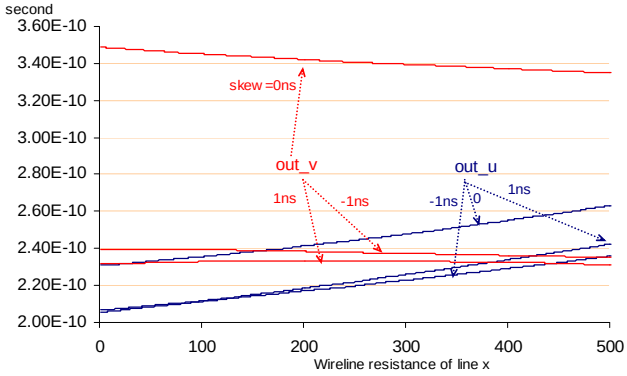


Figure 23: Transition times of out_u and out_v as a function of the wire resistance of line x for different input skew values.

P17: The crosstalk-affected output delay and transition time are weakly sensitive to the wire resistance value. In particular, they monotonically increase as the victim wire resistance increases (victim output: out_u) while monotonically decreasing as the aggressor wire resistance increases (victim output: out_v.) In both cases the effect can be well approximated by linear equations.

The reader is reminded that the range of the parameters has an important role in extracting the properties of crosstalk noise and its impact on circuit performance; it is sufficient to consider realistic ranges of parameters to reduce the complexity of analysis and modeling. The results presented previously are all qualified to the range of parameters considered during the simulation. These results can change if the parameter range is modified. To make this point more clear, let's suppose that the wire resistance of line x can range from 0 to 5kΩ (notice that the upper range is too high for typical interconnects in VLSI circuits.) The last two experiments (as reported in Figure 22 and Figure 23) are repeated with this extended wire resistance range and the results are provided in Figure 24 and Figure 25. Notice that the monotone behavior, which was observed for the reasonable range of wire resistances (0 to 500Ω), does not exist for this new range (0 to 5kΩ.)

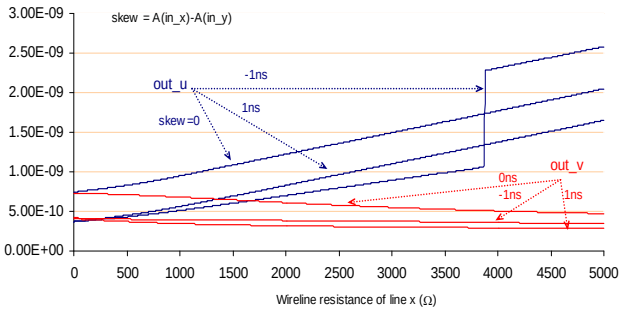


Figure 24: Delay from in_x (in_y) to out_u (out_v) as a function of the wire resistance of line x (ranging from 0 to 5kΩ) for three different input skew values.

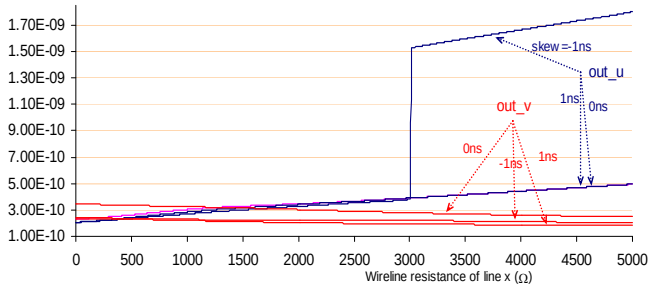


Figure 25: Transition times of out_u and out_v as a function of the wire resistance of line x (ranging from 0 to 5kΩ) for different input skew values.

5. CROSSTALK-INDUCED SPEEDUP

To study the crosstalk-induced speedup effect, we consider transitions with the same direction of change at inputs, in_x and in_y. We set the arrival time of a rising transition at in_y to 1000 ps and sweep the arrival time of a rising transition at in_x from -1000 to +1000 ps; therefore the input skew between in_x and in_y changes from -1000ps to +1000ps. We also set the input transition times to 100ps. Figure 26 illustrates the speedups that occur at outputs, out_u and out_v based on the input skew change. Figure 27 illustrates the output transition time vs. the input skew for the speedup case.

Having compared Figure 26 with Figure 3, we find that the maximum speedup at the victim's output is 233ps whereas the maximum slowdown was 390ps. Figure 5 and Figure 27 how that the maximum decrease in transition time at the victim's output is 110ps whereas the maximum increase in transition time for the slowdown case was 390ps. Hence, the amount of speedup for the same configuration is lower than the slowdown and the transition time change in the speedup case is less than that in the slowdown case. Since both lines make transitions in the same direction, the out_u and out_v curves are symmetric to each other. Other observations are similar to those of the slowdown ones.

Figure 26 and Figure 27 show that even for transitions in the same direction the zero skew may not create the worst case slowdown or output transition time. So P3 and P7 must be true even for completely balanced cells with equal rise and fall time transitions.

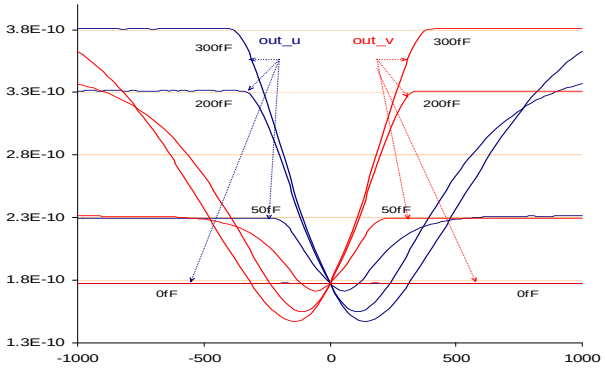


Figure 26: Delay from in_x (in_y) to out_u (out_v) as a function of input skew for different coupling values (speedup case.)

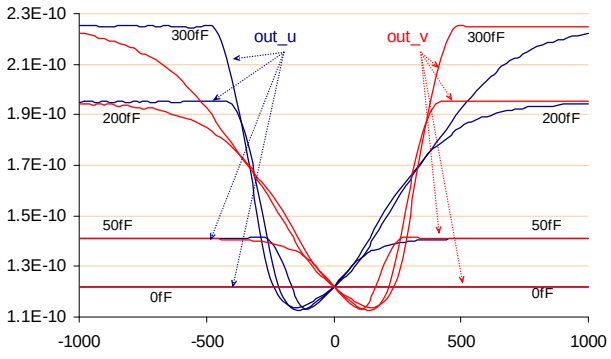


Figure 27: Transition time of out_u and out_v as a function of input skew for different coupling values (speedup case.)

6. DRIVER STRENGTH

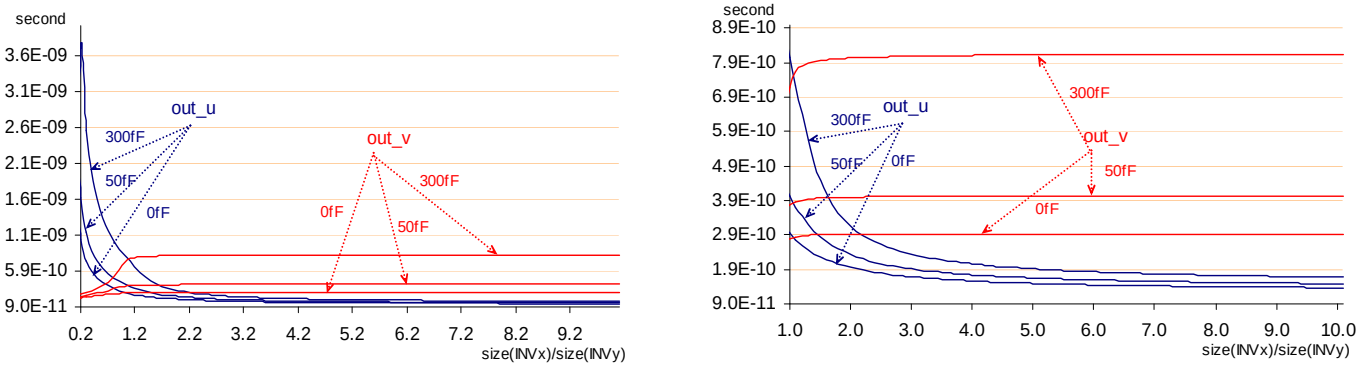
Driver sizing is considered as one of the most effective means of crosstalk reduction in optimization tools [20], [21]. In this section, we first study the effect of unbalanced cells on crosstalk noise and then do sensitivity analysis of this noise with respect to the driver strength.

6.1 Dependence on the Driver Strength

To study the behavior of the crosstalk-affected output delay as a function of the driver strength, the size of INV_y is kept constant, while that of INV_x is swept from 0.2 to 10 times the size of INV_y. Note that the size of the receiver $4INV_x$ and

4INV_y are kept constant at 4 times the size INV_y in this experiment; other parameters are set as explained in Section 2.1. Figure 28(a) shows the output delay versus the ratio of size(INV_x) to size(INV_y) for coupling capacitance values of 0, 50, and 300fF.

The driver sizing techniques usually attempt to take advantage of the trade-off whereby increasing the driver size aggravates the crosstalk effect for coupled lines. This trade-off is reasonable when a lumped RC modeling is applied in which the drivers are modeled as linear circuit elements. Considering line x as the victim line and line y as the aggressor line, Figure 28 confirms that the crosstalk-induced slowdown of out_u will decrease exponentially if the input driver size of the victim line is increased. It also shows that the crosstalk-induced slowdown of out_v is aggravated by an increase in the size(INV_x). However, the amount of slowdown aggravation at out_v is much less than (and almost negligible compared to) the slowdown decrease at out_u. This is more remarkable when noticing that the two lines are completely symmetric in everything but the size of the input drivers.

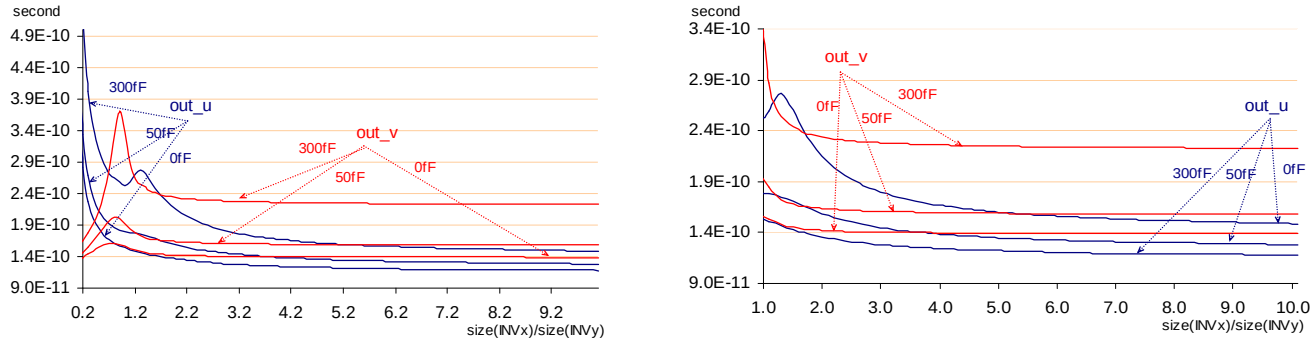


(a) (b) zoomed in the reasonable size ratio

Figure 28: Delay from in_x (in_y) to out_u (out_v) as a function of input driver size ratio.

Inspired by the typical concept of fanout-of-4 (FO4) for gate delay estimation, it is reasonable to assume that the driver size of an interconnect is at least ¼th of the size of its receiver, This implies that the minimum ratio of size(INV_x) to size(INV_y) is set to 1. With this sizing constraint, Figure 28(b) shows that the so-called trade-off may not be always valid. This is because the increase in crosstalk noise of the coupled line y is very small and quite negligible compared to the crosstalk reduction obtained in line x (even for a large coupling value of 300fF.) It is also worth noticing that increasing the driver size ratio beyond a certain point, say 4, can hardly change the crosstalk-affected delay. Figure 29 shows similar results for the transition time versus the driver size change. In this case a non-monotone behavior exists.

P18: Crosstalk-affected delay (transition time) at the output of the victim line receiver can be highly (moderately) sensitive to the driver strength of the victim line, but weakly sensitive to that of the aggressor line.



(a) (b) zoomed in for a reasonable sizing ratio

Figure 29: Transition times of out_u and out_v as a function of input driver size ratio.

6.2 Unbalanced Cells

So far we reported experiments on configurations with inverter cells with nearly equal rise and fall times. We call these cells *balanced*. To see how different rise and fall times may affect the results, we use driver and receiver inverter cells with different pulldown and pullup strengths. We refer to these types of logic gates as *unbalanced* cells. Figure 30 and Figure 31 show the delay and transition time change vs. input skew similar to configuration of Figure 3 and Figure 5 respectively, but with unbalanced cells used as line drivers and receivers. The falling transition at in_y occurs at +2000ps whereas the rising

transition at in_x occurs between 0 to +4000ps, i.e., the input skew changes from -2000ps to +2000ps. The delay value for very large negative or positive skews actually captures the delay of the interconnect output which is not affected by any crosstalk. For example, the delay of out_u for the skew of -2000ps is around 470ps and that for the skew of +2000ps is around 410ps. The difference between the two delay values is the delay of an interconnect line that is influenced by the voltage level of the other interconnect through the coupling capacitance.

P19: Crosstalk-affected delay and transition time at the output of the victim line receiver are highly sensitive to the ratio of pull-up and pull-down strengths of the inverter cells.

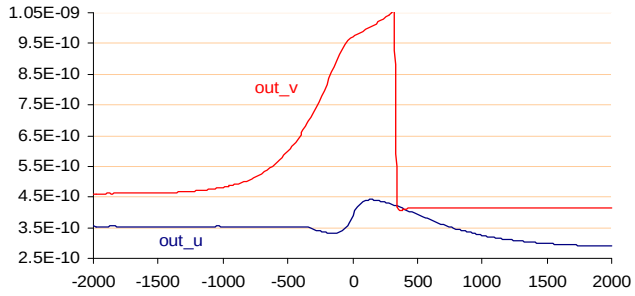


Figure 30: Delay from in_x (in_y) to out_u (out_v) as a function of input skew using an unbalanced cell.

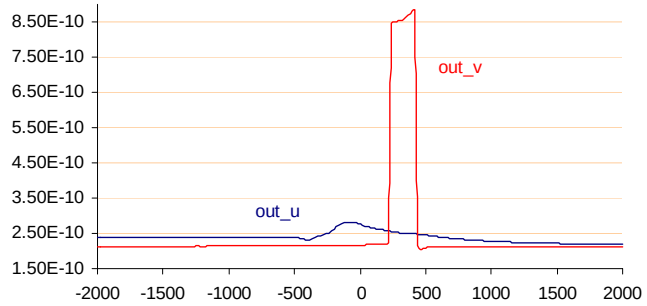


Figure 31: Transition times of out_u and out_v as a function of input skew for an unbalanced cell.

Figure 30 points out the non-monotone property of the crosstalk effect. Assume that the arrival time of in_x is sped up (e.g., as a result of the speedup effect of a crosstalk site in the transitive fan-in of node in_x) such that the input skew between in_x and in_y is reduced from 400 to 300ps. This skew reduction creates a 650ps increase in the crosstalk-induced slowdown at out_v. Now, looking at the same scenario in the opposite direction, we can see that an input skew increase from 300 to 400ps will reduce the delay at out_v by 650ps. So, in general, circuit scenarios can be found such that a speedup at the input line of a crosstalk site can result in either a speedup or a slowdown effect at the output of the site. Similarly, an input slowdown may cause an output slowdown or output speedup. In Section 7 we will further explore the impact of this non-monotone behavior when the crosstalk sites interact with one another.

P20: Crosstalk effect exhibits a non-monotone behavior with respect to the skew between the arrival times of the inputs of the aggressor and victim line drivers.

7. INTERACTION OF SITES

The crosstalk induced speedup or slowdown effects of two crosstalk sites, each similar to the one shown in Figure 1, may interact with each other if one is in the transitive fan-out of the other. In this section we show this interaction can generate a total delay effect that is more significant than the delay effects caused by each site in isolation.

7.1 Interaction of Two Slowdown Effects

Assume each has a total coupling value of 300fF. Assume both sites use the same moderately balanced cell that was used in Section 2.1 for all INV cells in the model. Consider a falling and a rising transition at the inputs in_x and in_y of the first crosstalk site. Figure 13 showed the slowdown effect vs. skew for this site. From Figure 13 a 30ps decrease in the arrival time of the transition at in_x of the first crosstalk site, which is equivalent to a 30ps increase in its input skew, can result in a slowdown of 150ps at out_u of this site. Let's consider a worst-case scenario where all of this slowdown effect will reach the input of the second crosstalk site. Referring to Figure 13, a 150ps change in input skew can cause an output slowdown of up to 400ps. Therefore the total slowdown along the path is 30+150+400 or 580ps. If we study the slowdown effect of the crosstalk sites one at a time, then we will incorrectly conclude that a 30ps change in the input skew of the site will create 150ps slowdown on each site, and thus to the total slowdown of the path is 30+150+150 or 330ps. Therefore, separate worst-case analysis of the two crosstalk sites would underestimate the total path slowdown by 93%. In addition, we should take into account the transition time change created at the output of the crosstalk sites. For example, in the case that one crosstalk site directly feeds into the other, from Figure 14, a 30ps change in the input skew causes a 90ps transition time change at the output of the first site and input of the second site. This in turn creates around 30ps extra slowdown at the output of the second site. This means that the total path slowdown is actually 580+30 or 610ps.

P21: Crosstalk sites along a path may result in a significant increase in circuit delay, which can be much higher than the summation of delay increases caused by each site individually.

7.2 Interaction of Slowdown and Speedup Effects

Assume a first site with total coupling value of 50fF uses the same moderately balanced cell that was used in Section 5 for all INV cells in the model. Assume rising transitions at the inputs of in_x and in_y of the first crosstalk site. Figure 26 showed the speedup effect vs. skew for this site. A 240ps decrease in the arrival time of the transition at in_x of the first site, which is equivalent to a 240ps increase in the input skew, can in the worst case cause a 60ps speedup at the output of the site. This speedup is in turn equivalent to a decrease in the input skew of the second site that is in the transitive fanout of the first one. The second site has a total coupling value of 300fF. It uses the unbalanced cell used in Section 6.2. Therefore, from Figure 30, a 60ps decrease in the input skew can create up to 650ps increase in slowdown. Therefore the total slowdown along the path is 240-60+650 or 830ps. Studying the second site in isolation, a 240ps increase in the input skew of the second site, which from Figure 13 means no slowdown at the output of this site, could be generated by the second site if the first site did not exist. The total slowdown created by each site in isolation is 240-60=220ps. Therefore the total slowdown caused by the interaction of site is more than 3.7 times as large as the summation of crosstalk effects in isolation. This example highlights the non-monotone behavior of crosstalk site described in P12.

The key to the synergistic interactions discussed in 7.1and 7.2 is that crosstalk-affected delay is highly sensitive to the input skew (refer to properties P3 and P7.)

8. SIDE-LOAD ROUTING

Consider the side-load of Figure 1(b); Assume it has to be routed in connection with line x. In the process it may be connected to any intermediate point along line x, i.e., out_x, sub1_x, … , or in_u. The question is which point gives the best performance in terms of crosstalk-affected delay. The following experiment was conducted to answer this question. We connected the side-load to out_x and then swept the size of the side-load, INV_{side} from 0.2 to 4 times the size of line x driver, i.e., INV_x. We repeated this experiment for the side-load connected to other intermediate points. Figure 32 and Figure 33 illustrate the output delay and transition time for both lines vs. the input skew for size(INV_{side}) equal to that of INV_x for three different coupling values (coupling values in the range 0 to 500fF showed similar behavior.)

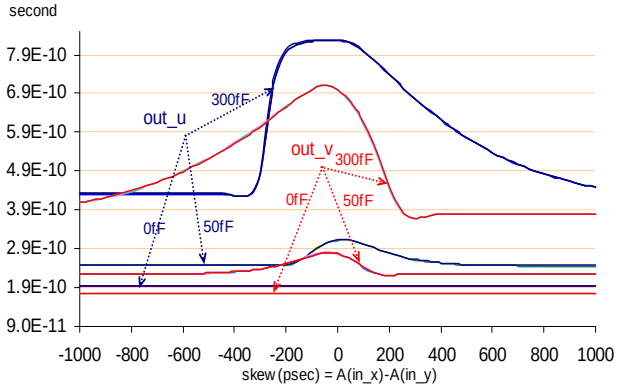


Figure 32: Delay from in_x (in_y) to out_u (out_v) as a function of input skew for different side-load connection points for coupling values 0, 50, and 300fF. size(INV_{side}) = size(INV_x.)

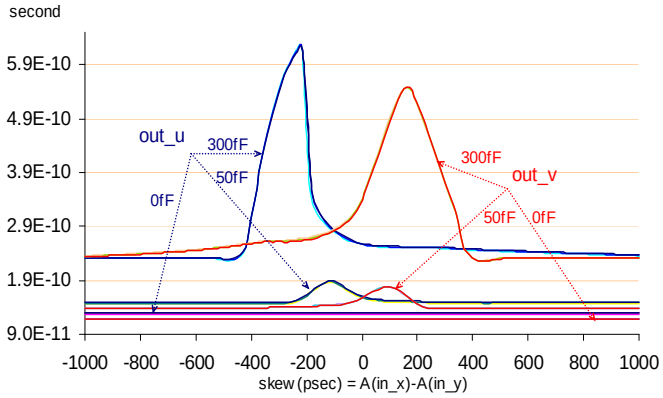


Figure 33: Transition times of out_u and out_v as a function of input skew for different side-load connection points for coupling values.

Figure 34 illustrates the delay for the case of size(INV_{side}) four times as large as that of INV_x, (the transition time figure is not shown since the results are similar to Figure 30.) Note that for a certain coupling value, the curves corresponding to different connection points almost fully overlap each other (actually hardly distinguishable from one another,) meaning that the connection point of the side-load of interconnect does not change the crosstalk-induced output delay (and transition time) of the interconnect.

P22: Crosstalk-affected output delay and transition time have zero sensitivity with respect to the connection point of the side-load.

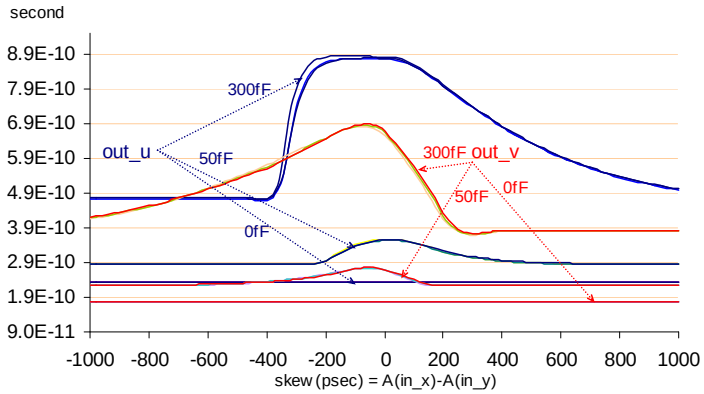


Figure 34: Delay from in_x (in_y) to out_u (out_v) as a function of input skew for different side load locations for coupling values 0, 50, and 300fF. size(INV_{side}) = 4 × size(INV_x.)

9. COUPLED INTERCONNECT – PROCESS VARIATION MODEL

9.1. Interconnect Sources of Variation

The variation of physical parameters, such as width and thickness along interconnect lines is in general due to the imprecision in the IC manufacturing process. This is in turn due to effects of the neighboring interconnect lines, non-uniform metal densities, Non-Linear Resistance (NLR) effect, Selective Process Bias (SPB) [22] effect, and thickness variation due to etching and CMP (Chemical Mechanical Polishing). Other sources of variation are die-to-die, wafer-to-wafer, lot-to-lot, and fab-to-fab variations. Thickness variation modeling is highly dependent on the accuracy of local wire density calculation [23]. The resultant model is expressed in terms of the size of a density box surrounding the critical wire segment. This box typically covers any neighbor wires that can influence the thickness of the critical wire segment. However, wires farther away from the critical wire segment do not contribute to the thickness variation as much as those which are closer. So a weighting function is applied by using a rectangular prism for modeling. The following can be used to compute the effective local density:

$$D_{eff} = \sum_i d(X_i) \cdot w(X_i) \qquad (9.1)$$

where Xi is the size of the density box of segment i, w(Xi) is its weighting factor, and d(Xi) is the density of the density box of segment i. The number of boxes, i (note that the number of boxed is equal to that of wire segments.) the size of the density box, Xi, and the w(Xi) are derived from silicon measurements by the semiconductor manufacturer's technology development group. The spatial correlation among the variation of neighboring segments is quite important in the crosstalk-induced delay of the victim interconnect. For example most of the variation resulting from chemical-mechanical polishing (CMP) of the inter-layer dielectric (ILD) is based on systematic spatial effects and vanes within-die [24].

The methodology proposed in this paper uses the spatial information to develop a systematic variation model of the coupled interconnects. The parameters corresponding to every pair of points on the interconnect line are correlated. The correlation relation is a function of distance between those two points. More precisely, for each physical parameter, p_i, (e.g., thickness), the correlation between the parameter values corresponding to two points along the interconnect length at locations x_1 and x_2 is as follows:

$$Corr(p_i(x_1), p_i(x_2)) = e^{-(x_1 - x_2)/L_{seg}} \qquad (9.2)$$

where $p_i(x_1)$ and $p_i(x_2)$ are the values of parameter p_i at locations x_1 and x_2 along the interconnect. L_{seg} is a predefined segment length that is assumed to be given to us. It is found by a series of characterization and extraction experiments by the manufacturer.

9.2. Statistical Model

To capture the effect of variations of physical parameters such as width, height, and interlayer dielectric thickness on the circuit metrics, the following two-step procedure is used for the calculation of electrical parameters of the distributed circuit model:

- *Physical outline generation*: Complete physical outlines of the coupled interconnect lines is generated in this step, including the information about their width, height, and interlayer dielectric thickness along their length and their correlation as described in section 9.1.

- *RC-π stage parameter calculation*: The generated physical outline of the coupled interconnects is used to calculate the corresponding electrical parameters for each interconnect segment.

The key advantage of the proposed modeling approach is the ability to locally capture the effect of process variations on each interconnect segment. This is done by directly calculating the corresponding values of local resistance and capacitance of the RC-π model based on the exact information about the actual geometry of the interconnect lines in each segment. This is in direct contrast with previous approaches [11]-[13], where a single sample of a given parameter is adopted from the corresponding distribution to extract the electrical parameters of the complete circuit model. Next, each interconnect line is divided to multiple segments of length, L_{seg}=100μm, and a set of parameters is randomly assigned to that segment based on the assumed distribution. To emulate the variations in the physical outline of the interconnect lines a Gaussian distribution is used for each physical parameter. The choices of distribution type, its characterizing parameters, and the correlations among physical parameters are based on the information made available from the semiconductor manufacturer as described in section 9.1. In the second step, parameter extraction scheme similar to [24] is used to calculate values of different electrical parameters in the RC-π model. Note that although the approach used for parameter extraction may lack absolute accuracy, it provides the required fidelity with respect to different physical dimensions. Moreover, since all of the experiments use the same extraction method, the presented results only capture the differences in the models, and are not impacted by the accuracy of the extraction procedure.

Figure 35 shows the line resistance and capacitance distribution of a segment of two 100μm-long coupled interconnect lines in metal-4. Note that none of these distributions are Gaussian, since the extraction procedures which transform the physical parameters of interconnect lines to the corresponding electrical parameters are non-linear, and therefore, they tend to result in non-Gaussian distributions for the electrical parameters. This is in contrast with the Gaussian-based assumptions used typically in statistical timing analysis methodologies [22], [25]. The best maximum-likelihood fit for these distributions are lognormal distributions, parameters of which are listed in Table 2 with confidence level of 98%. The corresponding fitted probability distribution functions (pdf) are shown by the red outlines in Figure 35.

It is mentioned in [22] that variations in electrical parameters of interconnect may be approximated as normal distributions with the exception of via and contact resistances which should be approximated as lognormal distributions. The Gaussian distribution assumption in this case is found to have and error of 3.5%.

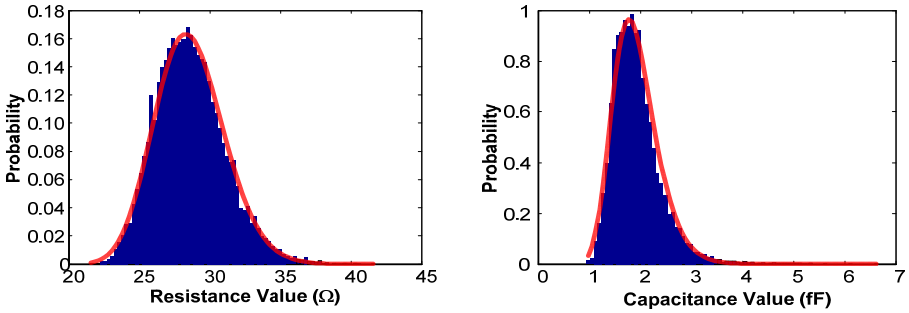


Figure 35: Resistive and Capacitive line distribution for a 0.1mm long metal-4 interconnect

	Resistance (Ω)	Capacitance (pF)
μ	3.3504	0.6271
σ	0.0861	0.2266

Table 2: The mean and standard deviation of the resistance and capacitance line variations depicted in Figure 35.

To simulate the crosstalk-affected delay of interconnect lines, a distributed circuit consisting of 10 RC-π stages are used (cf. Figure 36.) This is similar to the setup of Figure 2(a) with the difference that segments can have non-identical values. To capture the variations of each physical parameter, the two step procedure described in the beginning to this section is used to create a large population of samples for each physical parameter which in turn is transformed into the electrical parameters of the distributed RC-π model. Next, Hspice simulation is performed. To achieve convergence in the desired statistical properties of output variables, Monte Carlo simulation is performed. Based on normality assumption for the interconnect delay distribution, a sample size of 2500 is used i.e., the population generation and electrical parameter extraction steps are iterated 2500 times to achieve convergence in the desired statistical properties for each sample. The number of samples is then selected so that a 98% confidence level with 1ps error is achieved for mean and variance estimates.

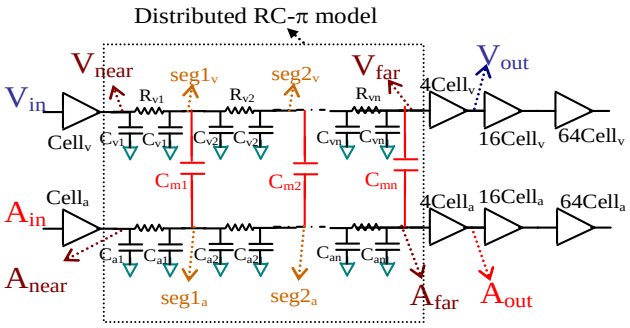


Figure 36: Distributed RC-π modeling of crosstalk site.

10. EXPERIMENTAL RESULTS

10.1. Statistical Comparison of Crosstalk Models

To show the necessity of a statistical approach, first the statistical model based on distributed RC-π circuit is compared against the conventional corner-based approach. As seen in Figure 37, the corner-based "μ+3σ" value of the victim delay is equal to 435ps which shows more than 46% pessimism compared to that in our statistical model with distributed circuit modeling (μ+3σ=290). As discussed earlier, the accuracy of the existing models for coupled interconnects can severely degrade in the existence of process variations. A goal of this work is to investigate the source of inaccuracies for some common crosstalk site models and try to resolve them. The single RC-π model, as well as the 2RC-π model of [26] are considered here as two such models.

The statistical distribution of the delay of the victim line for both approaches is illustrated in Figure 37. The mean delay is found to be very close to the one found by the distributed model (in fact the mean error for the single and two RC-π models is 5% and 3.2%, respectively.) However, the μ+3σ value for the single RC-π and 2RC-π is 330ps and 313ps respectively, meaning there is more than 13% and 7.9% pessimism in μ+3σ calculation when single and 2RC-π are used, respectively. This error mainly exists because when the extraction tool extracts the parameters values for each segment, it extracts the same value for each segment as long as the topology of the wire does not change; subsequently, these identical values are used by a model order reduction technique to create a reduced model such as the lumped RC or RC-π model. However, in reality the local process variations can cause parameter value variations in different segments (cf. section 9.1.)

10.2. Variation Shielding

To improve the accuracy of crosstalk models when used in a statistical analysis methodology, we propose the following heuristic algorithm. First, the interconnect line physical parameters are extracted based on conventional scheme. Next before applying the model order reduction formulas to find the capacitive or resistive value of each element in the reduced model with respect to those of each segment of the distributed model, we select the mean and variance of values in each segment as follows. The mean values for all segments are set to the extracted value. The variances are drawn from a family of distributions where their variances decrease geometrically as we proceed towards the far-end of interconnects. The reason behind this type of variance assignment is that based on extensive simulations, we have found that the variation of parameters in each segment is affected by a phenomenon that we refer to as *variation shielding*. By variation shielding, we mean that while moving from an interconnect driver towards the far-end of the interconnect line the effect of parameter value variations on the output delay is reduced. We model the variation shielding phenomenon for each parameter p by the following expression:

$$\sigma_p(\text{segment}_i) = \alpha \times \sigma_p(\text{segment}_{i-1}) \qquad (10.1)$$

where $\sigma_p(segment_i)$ is the variance of a parameter p of segment i. $1 \le i \le 10$ and $\alpha < 1$; α is set to 0.95 in our heuristic tool. Having selected the values for each segment, the model reduction is applied by using these modified values and the values of each circuit parameters in the reduced model specified.

We then repeat the experiments corresponding to Figure 37 using the values found through our heuristic. The results are shown in Figure 38. Compared to Figure 37, the pessimism is drastically reduced (e.g., for the case of 2RC-π model from 7.9% to 4% error in μ+3σ and from 3.2% to 1.4% error in mean, if α=0.95.) The intuitive reason is that the in case of the summation of the distributed parameters to a single value, the variations tends to cancel each other and thus the pessimism of the conventional approach for the extraction of a single component is reduced.

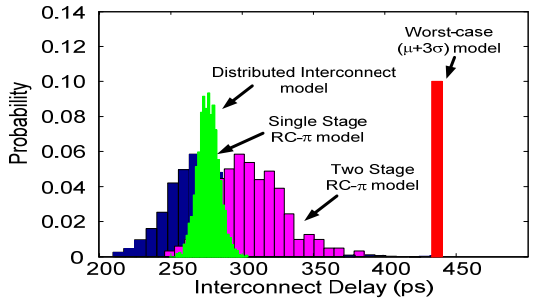


Figure 37: Comparison of different approaches with our statistical crosstalk model

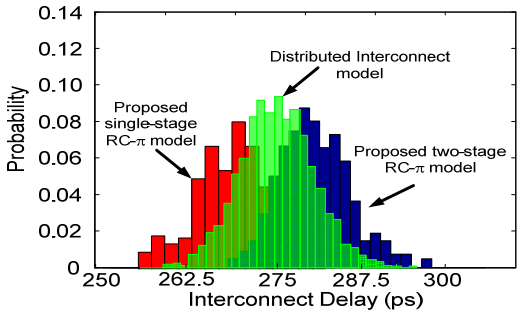


Figure 38: Accuracy improvement of 2RC- π crosstalk models.

10.3. Analytical Crosstalk-affected delay

The simulation setup of 3.2 is used to derive the mean and variance of crosstalk-aware output delay of the victim vs aggressor and victim line widths. They are shown in Figure 39 and Figure 40, respectively. Similar simulations have been performed considering different physical and electrical parameters. Each point in these figures is the result of 2500 sampled data in a Monte Carlo based environment. The large sampled data of 2500 points guarantees that the sample means have a normal distribution and that the closed form expression to model the effect of process variations on delay are accurate.

There is a tradeoff for the level of accuracy and complexity of closed-form expressions. As the number of input parameters increase, lower order models such as linear modeling of variation becomes more suitable. According to our experimental setup, we found the 2nd order modeling to be the most effective for the distribution properties of crosstalk-aware output delay and transition time of the victim line:

$$mean\ (delay\ ) = \sum_{parameter\ \ i} (A_i x_i^2 + B_i x_i) \qquad (10.2)$$

$$\text{var}\ iance\ (delay\ ) = \sum_{parameter\ \ i} (C_i x_i^2 + D_i x_i) \qquad (10.3)$$

$$mean\ (transition\ \ time\ ) = \sum_{parameter\ \ i} (E_i x_i^2 + F_i x_i) \qquad (10.4)$$

$$\text{var}\ iance\ (transition\ \ time\ ) = \sum_{parameter\ \ i} (G_i x_i^2 + H_i x_i) \qquad (10.5)$$

where coefficients A_i to H_i are empirically found by using our statistical analysis and curve fitting of the results.

To increase the efficiency of Equations (10.2) to (10.5.) we use the results of our extensive sensitivity analysis of crosstalk-affected delay to all circuit parameters (sections 2 to 8) to able to choose the right model (linear or higher order model) with respect to each parameter. For example a linear modeling is enough for the case of resistance and coupling values, however for wire capacitance a 2nd or higher order model is necessary. Figure 41 shows the fitted curve for the distribution of crosstalk-aware output delay of the victim line. To evaluate the accuracy of our statistical expressions, we tested many cases of coupled interconnects from various sections of an industrial design by using Hspice. We then compared the results with those found by using our statistical expressions. Figure 42 illustrates the corresponding results. The average and maximum error magnitude for the mean calculation of crosstalk-affected delay are 1.7% and 5.1% respectively. The corresponding errors for variance are 1.3% and 3.9% respectively.

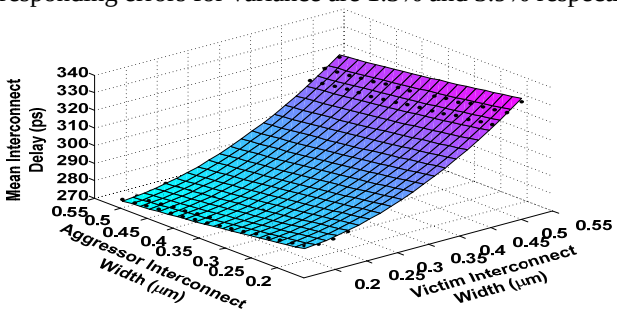


Figure 39: Crosstalk-aware victim interconnect delay (mean)

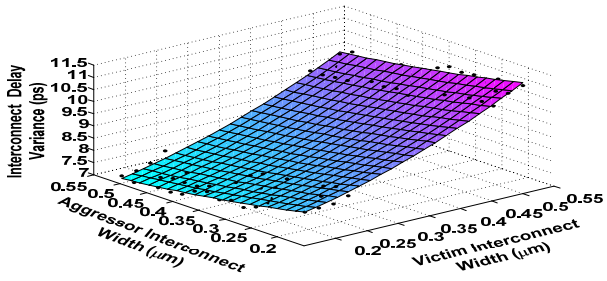


Figure 40: Crosstalk-aware victim delay (variance)

Performing Hspice-based study of the coupled interconnects while using the distributed RC-π model resolves the shortcomings of the previous approaches which rely on simpler, yet less accurate, circuit or waveform models. To increase the reliability of our statistical model, we had to simulate our circuit model under the whole range of physical parameters as well as variations in the input timing parameters, namely, skew and input transition times, for many coupled interconnects with different geometries. This kind of extensive simulation is required to be run only once per each process technology. The

resulting statistical crosstalk-affected delay expressions can subsequently be used throughout the whole design and testing stages.

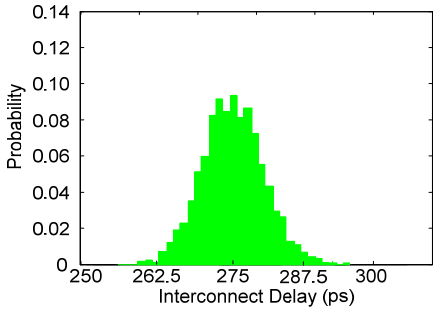


Figure 41: Crosstalk-aware output delay distribution for a 1mm long metal-4 interconnect pair

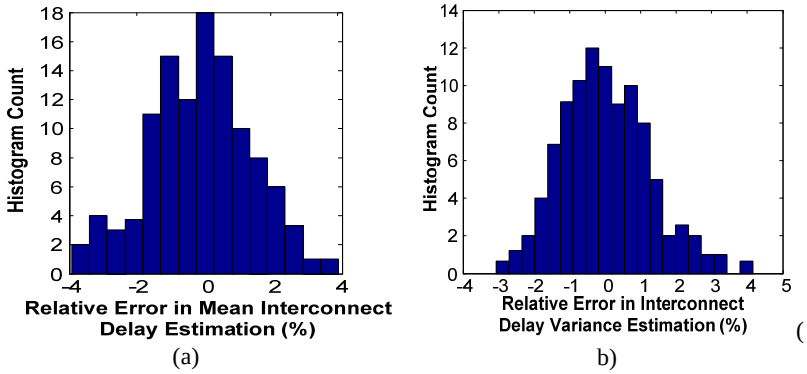


Figure 42: Accuracy comparison vs. Hspice a) Mean Interconnect delay b) Interconnect delay variance

11. CONCLUSIONS

We presented a number of key observations obtained from our extensive simulations of crosstalk-induce slowdown and speedup effects in TSMC 0.13µ process technology. The distributed modeling of capacitive coupling was used to create more realistic results compared to the previous work in the literature and industry. Table 3 summarizes the sensitivity strength of crosstalk effect to each parameter. Our sensitivity analysis shows the conventional assumptions based on lumped modeling regarding the monotone behavior of crosstalk with respect to wire capacitance may be invalid (P15 and P16.) It is however legitimate to assume a monotone property for crosstalk with respect to the coupling capacitance and wire resistance and apply linear modeling with respect to those parameters (P13 and P17.) We also performed some experiments and made some key observations regarding driver sizing and side-load routing, which are useful for crosstalk optimization purposes. For example we reported cases where increasing the driver size may not aggravate the slowdown of other coupled lines as envisioned by recent driver sizing algorithms (P18.) We also identified scenarios where the interaction of two crosstalk sites creates delay effects well in excess of the sum of their individual delay effects (P21.) We then proposed a statistical modeling to capture the effect of process variations on crosstalk-affected delay of coupled interconnects considering the large impact of correlation. A local process variation-aware distributed RC-π circuit modeling is developed for coupled interconnect pairs. Extensive Monte Carlo based Hspice simulations were to calculate the statistical properties of crosstalk with respect to variations in physical parameters and closed-form expressions for mean and variance have been derived. These expressions are shown to have near-to-Hspice accuracy. The effectiveness of this heuristic algorithm was confirmed for reduced models, namely, single and two RC-π crosstalk site models.

	Input Skew	Input Transition Time	Coupling Capacitance	Wire Capacitance	Wire Resistance	Victim Driver Strength	Aggressor Driver Strength	Pull-up to Pull-down Ratio	Side-Load Connection point
sensitivity	high	weak	high	Moderate	weak	high	weak	high	almost insensitive

Table 3: Crosstalk-affected output delay and transition time sensitivity to timing and circuit parameters.

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