Analysis of Power-Clocked CMOS with Application to the Design of Energy-Recovery Circuits*

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Abstract *— This paper presents our research results on power-clocked CMOS design. First we provide algebraic expressions and describe properties of clocked signals. Next two types of power-clocked CMOS circuit constructions are introduced and analyzed in detail. Since the adiabatic switching requires slow-ramping of the power-clock, a clocked transmission gate and a four-stage clocked NP-domino circuit are presented, which receive trapezoidal and sinusoidal power-clocks, respectively. PSPICE simulations demonstrate the correct operation and energy-saving advantage of the proposed circuits.*

I. INTRODUCTION

It is well known that the power dissipation in CMOS circuits is related to the type of energy conversion in the circuit. In static CMOS circuits, a DC power supply is used and the signal value is realized by charging/discharging of internal node capacitances. During this process, electrons are extracted from the V_{dd} terminal of the power supply, steered through the node capacitance, and returned to the ground terminal, resulting in an irreversible energy conversion from electric energy to heat. As a result, when a node capacitance is charged (or discharged), an energy dissipation of $\frac{1}{2}CV^2$ occurs [1]. So reducing the energy dissipation has been equated with reducing the *switched-capacitance*. Low power design targeting minimum switched-capacitance has made significant progress in recent years. [2] Researchers and designers however remain interested in developing logic elements that operate based on a different type of energy conversion, i.e., one that minimizes the conversion of electric energy to heat.

An energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e., electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e., magnetic field energy, into the digital circuit. If we relate the signal change to the conversion of electric energy to magnetic energy, the irreversible conversion from electric energy to heat caused by dissipative elements, i.e., resistors is largely avoided. For this reason, researchers have attempted to make a breakthrough in low-power CMOS circuit design, from basic circuit unit to microprocessor, by changing the mode of energy conversion. [3-7]

Energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be alternating quantities. The latter has been extensively used in dynamic CMOS logic, clocked CMOS logic, and various domino logic.[1] However, these circuits still rely on DC power, and the energy conversion remains as electric energy to heat. Therefore, we should further study the case of circuits supplied with the AC power. Since the AC power controls the working rhythm of the circuit and acts as the clock at the same time, it has been called the *power-clock*.[8]

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In this paper, we investigate CMOS circuits, which adopt a power-clock and use clocked signals. In section II, the algebraic expressions and the corresponding properties of clocked signals are discussed. In section III, various CMOS gate circuit constructions, which adopt a power-clock, are presented and analyzed. Logic waveform constraints on the power-clock and the clocked signals are analyzed and the suitability of two clocked CMOS gate circuit constructions is verified in section IV. Furthermore, the clocked transmission gate and the NP domino circuit adopting a trapezoidal power-clock and a sinusoidal power-clock are analyzed in section IV. Section V concludes the paper.

II. AN ALGEBRA FOR CLOCKED SIGNALS

From now, we assume that the clock is a symmetric square-wave. When $clk = 1$, the clocked signal displayes its true logic value; when $clk = 0$, the clocked signal is forced to its "base" value, 0 or 1. For the precharge circuits, the base value is 1 whereas for the predischarge circuits, the base value is 0. Therefore, in every clock cycle, the clocked signal is divided into two stages: set base (B) when $clk = 0$ and evaluate (E) when $clk = 1$.

Figure1 shows a pair of complementary signals $x / \bar{x}$ and the corresponding clocked signals. The values of $x / \bar{x}$ in Fig.1 are (101101)/(010010) and can be regarded as the synchronous outputs of a falling edge-triggered flip-flop. $x / \bar{x}$ are however not clocked signals. In Fig.2, $x^{\cdot clk}$, $\bar{x}^{\cdot clk}$, $x^{+\overline{clk}}$ and $\bar{x}^{+\overline{clk}}$ are four clocked signals derived from $x / \bar{x}$. Notice that the superscript i in the exponent expression of x^i, $i \in \{\cdot clk, +\overline{clk}\}$, represents the logic relation between the original signals $x / \bar{x}$ and $clk / \overline{clk}$. That is, $x^{\cdot clk}$ is $x \cdot clk$, $x^{+\overline{clk}}$ is $x + \overline{clk}$, and so on. Obviously, the function of $(\cdot clk)$ and $(+\overline{clk})$ is to set the clocked signal during the B stage to base "0" or "1", respectively.

The following inverting relationships exist among the four clocked signals (cf. Fig.1):

1. Logic value inverse (with the same base), such as $x^{\cdot clk}$ and $\bar{x}^{\cdot clk}$; $x^{+\overline{clk}}$ and $\bar{x}^{+\overline{clk}}$.
2. Base inverse (with the same logic value), such as $x^{\cdot clk}$ and $x^{+\overline{clk}}$; $\bar{x}^{\cdot clk}$ and $\bar{x}^{+\overline{clk}}$.
3. Complete inverse, such as $x^{\cdot clk}$ and $\bar{x}^{+\overline{clk}}$; $\bar{x}^{\cdot clk}$ and $x^{+\overline{clk}}$.

Figure 1 also shows that:

$$\overline{x^{\cdot clk}} = \bar{x}^{+\overline{clk}}, \quad \overline{\bar{x}^{\cdot clk}} = x^{+\overline{clk}}. \tag{1}$$

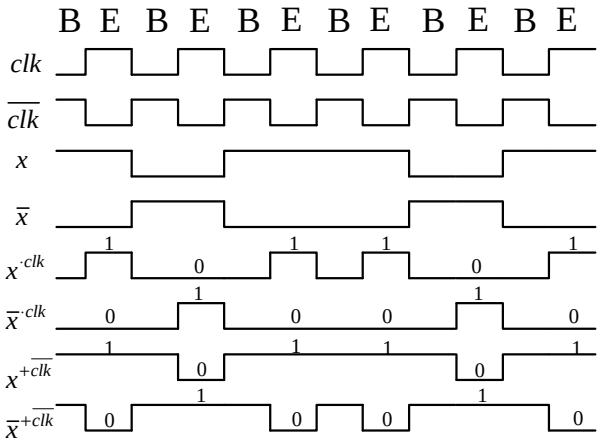

Figure 1 Four clocked signals derived from signal *x*.

In line with the above-mentioned exponent expressions, the power supply V_{dd} (1), the ground (0) and the clock ($clk / \overline{clk}$) satisfy the following clocked expressions:

$$1 = 1^{+\overline{clk}},\ 0 = 0^{\cdot clk} \tag{2}$$

$$clk = 1^{\cdot clk},\ \overline{clk} = 0^{+\overline{clk}} \tag{3}$$

If we regard the exponent operation as a Boolean operation, then Eq.(2) and Eq.(3) can be easily proved. Furthermore, we can also prove the following laws:

$$(x \cdot y)^{\cdot clk} = x^{\cdot clk} \cdot y^{\cdot clk},\ (x \cdot y)^{+\overline{clk}} = x^{+\overline{clk}} \cdot y^{+\overline{clk}} \tag{4}$$

$$(x + y)^{\cdot clk} = x^{\cdot clk} + y^{\cdot clk},\ (x + y)^{+\overline{clk}} = x^{+\overline{clk}} + y^{+\overline{clk}} \tag{5}$$

Eq.(1)—Eq.(5) can be physically explained as follows:

1. Eq.(1) represents the De Morgan's Law. It shows that the inverter function applied to clocked signals produce the complete inverse of the original clocked signals.
2. Eq.(2) shows V_{dd} (1) and ground (0) can continually work in the clocked circuits of base 1 and base 0, respectively.
3. Eq.(3) indicates that *clk* can assume the role of power supply in the clocked circuit of base 0, whereas $\overline{clk}$ can assume the role of ground in the clocked circuit of base 1.
4. Eq.(4) and Eq.(5) suggest that the clocked signals which participate in the AND/OR operations, should have the same base. Furthermore, the result is equal to the AND/OR operations of the original signals, then clocked by the same base. We should point out that the result of NAND and NOR operations inverts the base Eq.(1).

III. CLOCKED CMOS GATE CIRCUITS

From the discussion in the previous section, we see that the clocked signals are obtained by ANDing/ORing the original signal *x* with $clk / \overline{clk}$. However, the clocked signals can be realized with simpler circuits, as shown in Fig.2(a) through Fig.2(d). Notice that Fig.2 (c) and Fig.2 (d) are the precharge circuit and the predischarge circuit of dynamic CMOS logic. When $clk = 0$, these two circuits set the output to base-1 and base-0; when $clk = 1$, they evaluate the output according to input *x*. The output terminal may be put in suspension (high-impedance) state during the evaluate stage if the evaluation MOS transistor is off. In this case, the output value is determined based on the charge stored on the load capacitance.

If instead we use $clk / \overline{clk}$ to replace the power and ground in Fig.2 (c) and Fig.2 (d), then we obtain the circuits in Fig.2 (e) and Fig.2 (f). The reader can easily verify that the two power-clocked gate circuits work correctly and produce the desired output (cf. Observation 3 of section II).

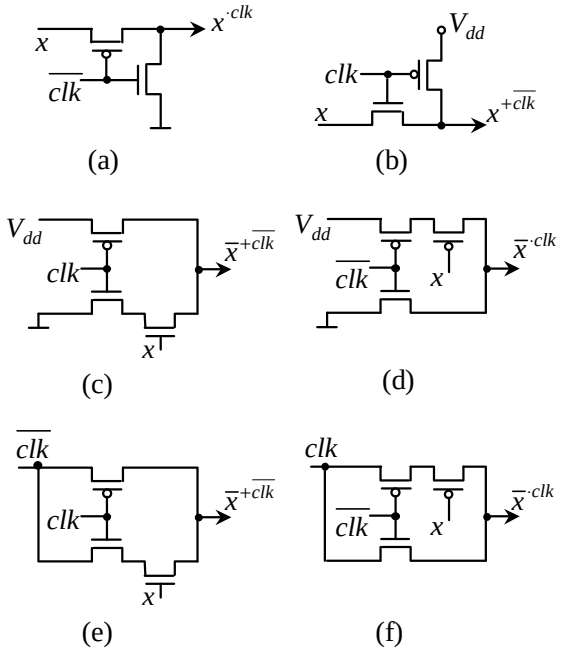

Figure 2 Circuit realizations of clocked signals.

Generally, the input signal for the circuits in Fig.2 is the clocked output signal of a preceding clocked CMOS gate. For the circuits of Fig.2(a) and Fig.2(b), if the input signal is in suspension state during the evaluate stage of the current circuit, then turn-on of the local MOS transistor will redistribute the charge which was originally stored in the input node capacitance and the node voltage will thereby be corrupted. Therefore, the circuits in Fig.2(a) and Fig.2(b) cannot be used in this case. Note that the circuits in Fig.2(e) and Fig.2(f) do not suffer from the unwanted charge redistribution problem. Besides, if they are cascade-connected to form a NP-domino connection, then the evaluation transistors will not turn on during the base set. Consequently, the MOS transistors that are connected in series with the evaluation transistors can be omitted.

Based on the above analysis, we present four types of clocked CMOS circuits as shown in Fig.3. In the traditional transmission gate, a source signal is transmitted and the output signal reproduces any change on the input signal. In Fig.3 however the transmitted source signal is the power-clock $clk / \overline{clk}$. Also note that in Fig.3(a) and Fig.3(b), the control signals of the transmission gates are complete inverse of one another. The base-0 and base-1 clocked signals act on the pMOS transistor and nMOS transistor, respectively. This guarantees a perfect transmission. The operational principles of these two circuits can be understood by examining the waveforms depicted in Fig.1. We note that when *clk* is transmitted, the output is a base-0 clocked signal and logic-inverse of the base-0 control signal on the pMOS transistor. When *clk* is transmitted, the output is a base-1 clocked signal and the logic-inverse of the base-1 control signal on the nMOS transistor. Therefore, the circuits in Fig.(a) and (b) act as logic-inverters. As to the circuits of Fig.3(c) and Fig.3(d), they also have the form of transmission gate. However their control signals are not complementary, thus they are still precharge and predischarge type circuits. Notice that each output is the complete-inverse of its input in these circuits.

We have shown in Fig.3 that given any two of the four complementary clocked signals, the other two clocked signals can be generated. The input transistor (or evaluation transistor) receiving the input clocked signal may be expanded to any MOS transistor network, thereby a type of clocked CMOS circuit, which

has a more complicated logic function, may be achieved. In Fig.4 we show the circuits to realize the clocked signals of $f = \overline{x \cdot (y+z)}$. In Fig.4(b) the connection is easy to understand. In Fig.4(a) the output can be expressed as $\overline{x}^{\cdot clk} + \overline{y}^{\cdot clk} \cdot \overline{z}^{\cdot clk}$. Other similar clocked circuits can easily be derived.

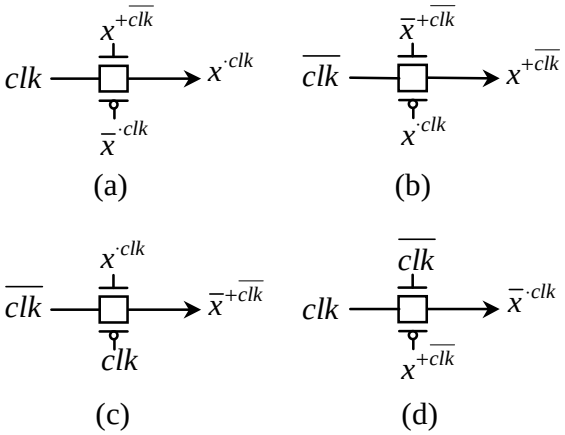

Figure 3 Clocked CMOS gates.
(a) clocked transmission gate for base-0 signal
(b) clocked transmission gate for base-1 signal
(c) n-logic precharge circuit
(d) p-logic disprecharge circuit.

IV. SLOW-RAMPING POWER-CLOCK AND ENERGY-RECOVERY CIRCUITS

We have pointed out in Section I that one-way transmission of charge from the positive pole of the power supply (V_{dd}) to the negative pole (*Gnd*) will lead to an irreversible energy conversion from electric energy to heat (i.e., energy dissipation). In Section III, instead of using the DC power supply and ground, we adopted the power-clock in the circuits of Fig.3 to charge the output node and receive back the charge from the node capacitance. This reversible charge transmission provides the basis for the design of energy-recovery circuits. Because of the turn-on resistance of the transistor which lies in the path of charge transmission, the conversion from electric energy to heat (and hence energy dissipation) still exists. For this reason, we should carry out the energy dissipation analysis for the charging and discharging processes.

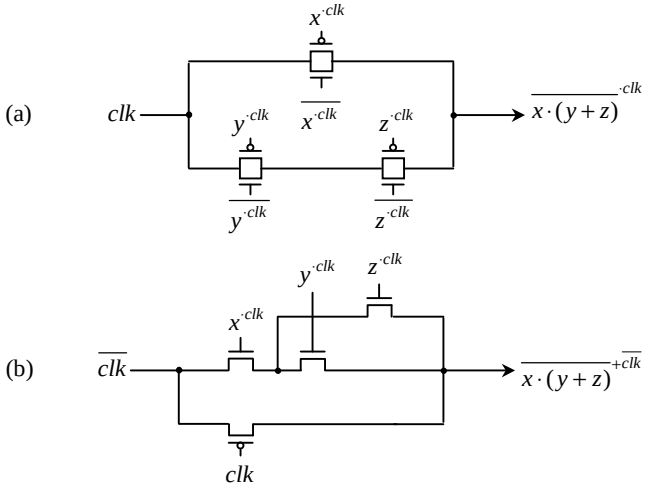

Figure 4 Clocked CMOS circuits for realizing $f = \overline{x \cdot (y+z)}$.
(a) clocked transmission gate, (b) n-logic precharging circuit.

Take the charging process as an example, during a period of 0→T, $V_c(t)$, the voltage of the node capacitance, starts at low-level $V_c(0) = 0$ and is charged to high-level $V_c(\mathrm{T}) = V_{dd}$. Suppose that the voltage of power supply is a function of time: $V_d(t)$, we have $V_d(\mathrm{T}) = V_{dd}$. Furthermore, the charging current flowing through the MOS transistor network is also the function of time: $i(t)$. So the energy converted into heat in this process is:

$$\begin{aligned} E_{dis} &= \int_0^T i(t)[V_d(t) - V_c(t)] \cdot dt \\ &= \int_0^T i(t) V_d(t) dt - \int_0^T i(t) V_c(t) dt = E_1 - E_2 \end{aligned} \qquad (6)$$

In Eq.(6), E_1 is the total energy injected in the circuit during the process, E_2 is the final energy stored in the node capacitance when the charging process ends. Because the current $i(t)$ and the voltage $V_c(t)$ of the capacitance have the following relation:

$$i(t) = c \frac{dV_c(t)}{dt} \qquad (7)$$

E_2 is easily obtained by integration, $E_2 = \frac{1}{2} C V_{dd}^2$. If we place Eq.(7) into Eq.(6), we get E_1 as,

$$E_1 = \int_0^{V_{dd}} C \cdot V_d(t) \cdot dV_c(t) \qquad (8)$$

If V_d is constant: $V_d(t) = V_{dd}$, then $E_1 = C V_{dd} \cdot \int_0^{V_{dd}} dV_c(t) = C V_{dd}^2$. From Eq.(6), the energy dissipation in the charging process of this node is: $E_{dis} = \frac{1}{2} C V_{dd}^2$. However, if $V_d(t)$ rises gradually (ramps up) from 0 to V_{dd} during the period of 0→T, and this rising process is slow enough to make the capacitance's voltage $V_c(t)$ track the change of $V_d(t)$: $V_c(t) \approx V_d(t)$. From Eq.(8) we get $E_1 \approx \frac{1}{2} C V_{dd}^2$, thus $E_1 \approx E_2$. So $E_{dis} \approx 0$ in Eq.(6). That is to say that there is almost no energy converted into heat for the nodes in the corresponding charging process. Similarly, the discharging process of node capacitance can be analyzed. Finally, a conclusion is obtained. So long as we adopt a ramping power supply and the voltage of node capacitance tracks the change of power supply during the charging and discharging process, the energy converted into heat is reduced to zero.

Based on the above discussion, the power-clock in circuits of Fig.3 should not have very short rising and falling times. As an extreme example, if we use a rectangular power-clock whose rising and falling times are zero, this result is equivalent to using a constant DC power supply and no energy saving will be obtained. Basically, previous researches have adopted either a trapezoidal power-clock or a sinusoidal power-clock. The first is easy to analyze but difficult to generate. As to the sinusoidal power-clock, the general RLC circuit can produce the resonant clock, so it has higher practical significance. Since we now use the slow-ramping power-clock, the correctness of the circuits that used a rectangular power-clock in the last section should be verified. We do this next.

4.1 Power-clocked transmission gate

If the output can track the changing of input signal, the transmission gate is a good choice for the adiabatic operation. Reference [4] proposed an adiabatic circuit by using transmission gates, as shown in Fig.5(a). This circuit has a simple structure. (The two clamp nMOS transistors are used to avoid the output terminal from floating and may be omitted.) We notice that in this circuit only base-0 signals are used, thus the control signals, $x^{\cdot clk0}$ and $\overline{x}^{\cdot clk0}$, on nMOS and pMOS transistors are logic inverse, rather than complete inverse, of one another. If the original power-clock used in the previous stage, clk_0, is taken as the local power-clock, then it cannot be transmitted correctly. Thus in this circuit, another power-clock with a shorter width, clk_1, should be used. The waveform obtained from PSPICE simulation is shown in Fig.5(b), where the trapezoidal power-clocks are used. It is seen that the transmitted signals $x^{\cdot clk1}$ and $\overline{x}^{\cdot clk1}$ have the same logic function, but a shorter width compared with $x^{\cdot clk0}$ and $\overline{x}^{\cdot clk0}$. By connecting the transmission gates in series or in parallel, more complex logic functions can be realized.[7] Computer simulation using PSPICE with 2 μ CMOS parameters also proves that this circuit has low energy consumption during its operation. However, the need for retractile power-clocks is a shortcoming that makes the circuit less useful in practice.[8]

Instead we take the clocked CMOS circuit of Fig.3(a), which also uses a transmission gate, to construct the circuit in Fig.6(a). When using a trapezoidal power-clock, we simulated the circuit of Fig.6(a) by PSPICE with 2 μ CMOS parameters. The result is shown in Fig.6(b). As was discussed for Fig.3(a) and Fig.3(b), the base-0 and base-1 clocked signals acting on the pMOS and nMOS transistors guarantee perfect signal transmission. Therefore, no retractile power-clocks are needed in the circuit. However, it is found that the output node does not maintain a flat top or bottom when the transmission gate shuts down. This can be explained as follows. Take $x^{+\overline{clk}}$ as an example. clk does not immediately jump to high-level when $x^{+\overline{clk}}$ is dropping; Furthermore, the nMOS transistor in the transmission gate is still turn-on at that moment, so the output tracks clk and rises until the nMOS transistor shuts down completely. This phenomenon affects the noise margins, but detailed simulation has proved that it does not affect correct transmission, as shown in Fig.6(b). Figure 6(c) depicts the energy dissipation waveform of the trapezoidal power-clock and the DC power supply when the input sequence pair (01010) and (10101) are used. A comparison between the two energy dissipation curves demonstrates the extent of energy recovery. Indeed the power-clocked circuit consumes only about 14% of energy dissipation of the conventional circuit.

As another example, we also verify the clocked circuits in Fig.4(a) by using a trapezoidal power-clock. If the inputs are x (01010101), y (00110011) and z (00001111), the PSPICE simulation result in Fig.7 shows that output f has the correct response: (11101000).

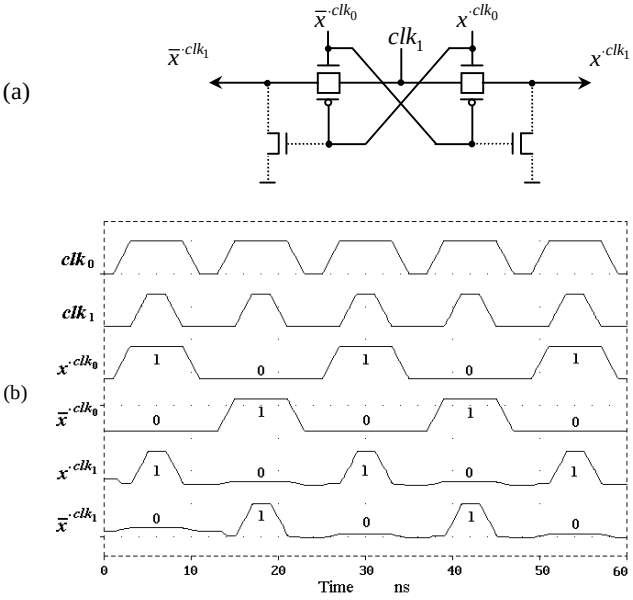

Figure 5 Simulation of the adiabatic transmission gate of reference [4] using a retractile trapezoidal power-clock.
(a) circuit, (b) output waveforms.

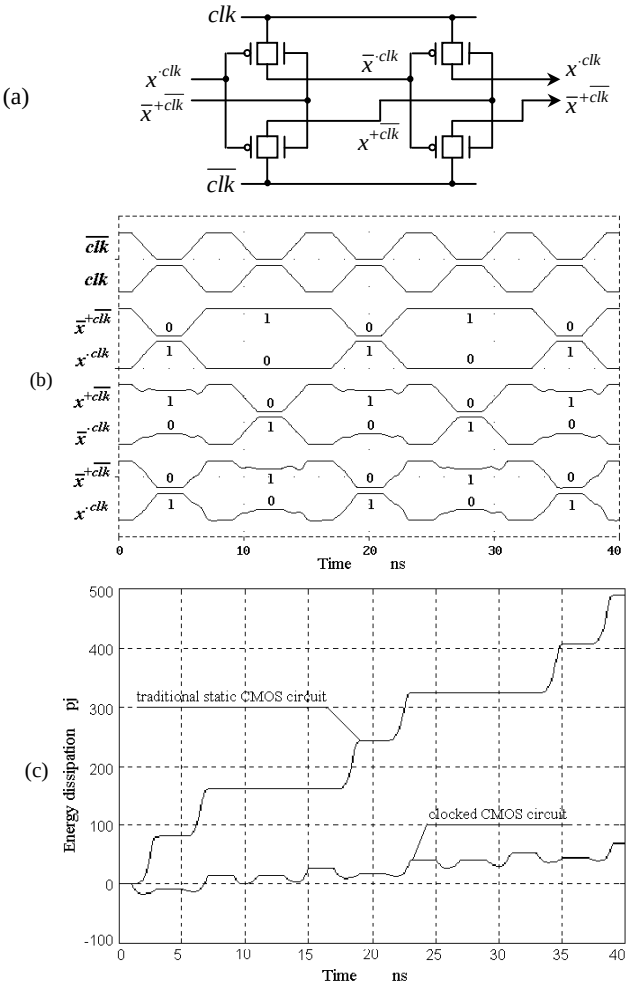

Figure 6 Computer simulation of the proposed transmission gate by using a trapezoidal power-clock.
(a) circuit, (b) output waveforms, (c) energy dissipation waveform.

4.2 Power-clocked NP domino circuit

We now verify the clocked CMOS circuits of Fig.3(c) and Fig.3(d) by using a sinusoidal power-clock instead. A power-clocked four-stage NP domino circuit shown in Fig.8(a) is constructed and simulated by PSPICE with 2 μ CMOS parameters using an alternating input sequence (10101…). The output waveform of each inverter $V_1 \cdot\cdot V_4$ is shown in Fig.8(b). To see the relationship between the output and the power-clock, we superimpose the power-clock (in dotted line) on each output waveform. It is seen that each output waveform has a small protrusion with respect to corresponding power-clock in the evaluation stage. This is caused by an imperfect signal transmission since the control signals on the MOS transistors are changing during the charging and discharging of the node. A further simulation proved that this protrusion does not affect the recognition of the corresponding logic value, even after cascading a large number inverting stages. This protrusion however results in some energy dissipation (see Fig.8(c)) which makes the circuit only "partially adiabatic" (semi-adiabatic).

We compare the power-clocked four-stage cascade domino circuit with four series connected static CMOS inverters in terms of the power dissipation. Figure 8(c) depicts the energy dissipation waveform of the sinusoidal power-clock and DC power supply when the input sequence is (10101…). The lower waveform demonstrates the energy recovery in the clocked NP domino circuit. It is seen that the four-stage cascade NP domino circuit, which adopts a sinusoidal power-clock, saves about 73% of the energy of the traditional circuit. These comparisons prove that the goal of reducing energy dissipation can be achieved by using the clocked CMOS circuits with gradually rising and falling power-clocks.

V. CONCLUSIONS

Clocked CMOS circuits, which use slow-ramping power-clock, can result in a considerable energy saving. Many researchers have studied this issue in recent years.[3-15] However, the operational constraint that the output signal should track the power-clock's slow-ramping behavior to accomplish the charging and discharging processes creates a major difficulty in the circuit design. Furthermore, the input signal should be valid when the local output tracks the rising and falling behavior of the power-clock. This implies that either a retractile power-clock scheme (as was discussed in previous sections) or a multi-phase power-clock should be used. In the latter case, a multi-phase power-clock ensures that different clock phases are used for the input action and the output evaluation. [9-15] Now if the output remains valid after the input has gone invalid, the device is performing a memory function, whether or not we intended it.[8] Consequently, when the current input acts on the circuit, the output will not be effective until the next phase. Therefore, although the designed circuit has a valid logic function, its applicability is limited.

We believe that research on novel design of adiabatic gates which do not suffer from the above-mentioned shortcomings is fundamental to the success and wide use of adiabatic circuit elements by digital circuit designers.[3,5,7] Thus our work focused on the design of adiabatic circuits, which do not require a retractile power-clock or a multi-phase power-clock. The present paper thereby presented a systematic study of clocked signals using an appropriate algebra. From this perspective, the construction of clocked CMOS gate circuits based on power-clock was investigated. Two new types of energy-recovery CMOS circuits, the clocked transmission gate supplied by a trapezoidal power-clock and a four-stage NP-domino circuit supplied by a sinusoidal power-clock, were designed and simulated with PSPICE and demonstrated to have correct logic functionality and sizable energy saving. Although these circuits do not achieve the ideal adiabatic result, they attain energy savings of 86% and 73%, respectively compared to their static counterparts.

In this paper, we only considered design of combinational logic circuits based on the power-clock. Reference [13] describes a CMOS flip-flop using the power-clock, which is constructed by cross-coupling the circuits shown of Fig.3(c). By using this flip-flop along with the power-clocked circuits proposed in this paper, the low-power clocked CMOS sequential circuits can be realized.

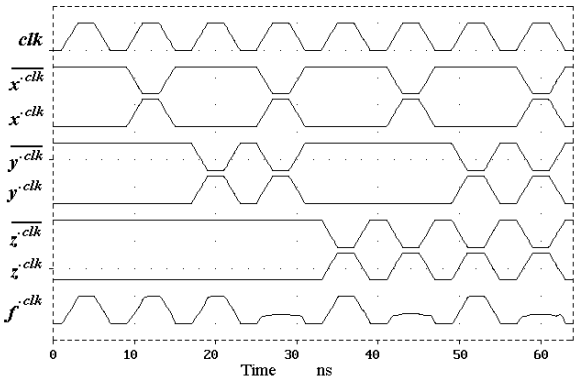

Figure 7 Simulation of circuit in Fig.4(a) by using a trapezoidal power-clock.

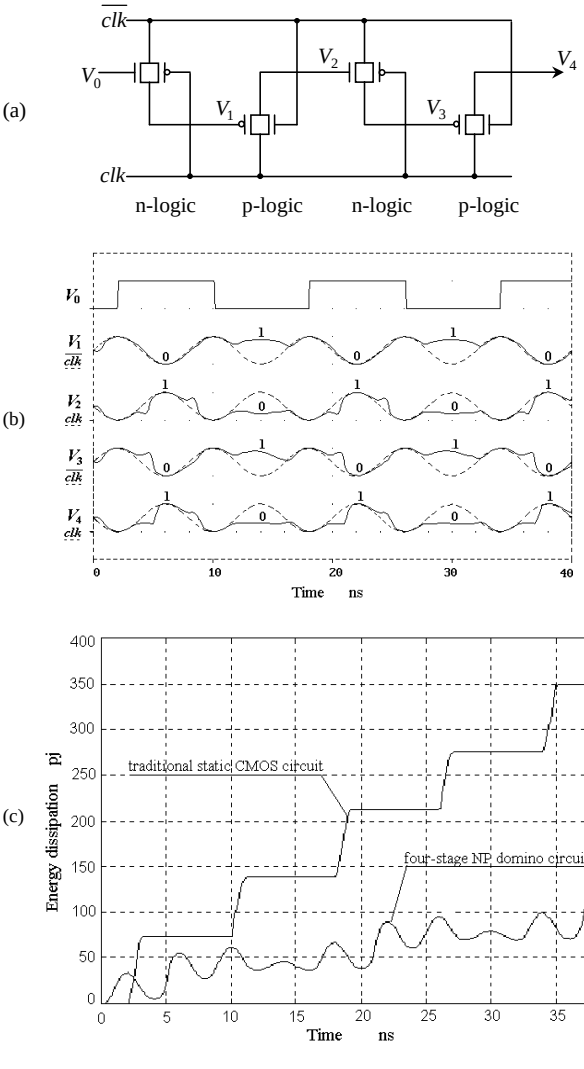

Figure 8 Simulation of four-stage NP domino circuit using a sinusoidal power-clock.

(a) circuit, (b) output waveforms, (c) energy dissipation waveform.

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