Parameterized Block-Based Non-Gaussian Variational Gate Timing Analysis

Soroush Abbaspour, Hanif Fatemi, and Massoud Pedram
University of Southern California
Department of Electrical Engineering
Los Angeles CA

Abstract

As technology scales down, timing verification of digital integrated circuits becomes an extremely difficult task due to the gate and wire variability. Therefore, statistical timing analysis (denoted by σTA) is becoming unavoidable. In this paper, two new approaches for doing statistical gate timing analysis for Gaussian and non-Gaussian sources of variation in block-based σTA are presented. To start, a variational RC-π load is approximated by using a canonical first-order model. Next, an accurate variational gate timing analysis (VGTA) technique, which accounts for variational *RC*-π loads, statistical input transitions, and a variation-aware gate library, is introduced. The proposed method relies on a novel static effective capacitance calculation method and its variational form. Experimental results demonstrate that VGTA exhibits an average error of only 4% for gate delay and output transition time with respect to the Monte Carlo simulation with 10^4 samples. Next, a more efficient variational gate timing analysis (called F-VGTA) based on a single-iteration variational effective capacitance calculation is presented. Experimental results show F-VGTA achieves an average error of 7% for gate delay and output slew time with respect to the Monte Carlo simulation with 10^4 samples, but with runtimes that are about two times faster than VGTA.

* This paper combines and extends results of our works, which were presented at the 2005 International Conference on Computer Design and the 2006 Asia-South Pacific Design Automation Conference.

1. Introduction

Process technology and environment-induced variability of gates and wires in VLSI circuits makes timing analysis of such circuits a challenging task [1]. More precisely, advanced analysis tools must be developed which are capable of verifying the changes in the circuit timing that stem from various sources of variations. These sources are in turn due to the following: imperfect CMOS manufacturing processes (e.g., variations in L, T_{OX}, V_T or ILD thickness), environmental factors such as drops in V_{dd} (resistive drop and ground bounce), substrate temperature changes (due to migration of local hot spots over the chip area), and device fatigue phenomena (e.g., electro-migration, hot electron effects, and negative bias temperature instability) [2].

σTA approaches can be classified into two major groups: path-based and block-based. . In the path-based algorithms, a selected set of paths is submitted to the statistical timer for detailed analysis. Path-based statistical timing is accurate and has the ability to realistically capture correlations, but suffers from other weaknesses. For instance, it is not clear how to select paths for the detailed analysis since one of the paths that is omitted may be critical in some part of the process space. In addition, path-based statistical timing often does not provide the diagnostics necessary to improve the robustness of the design [2]. Due of shortages of path-based σTA, block-based σTA has received a lot of attention. In block-based σTA, every timing quantity of interest (e.g., delay and slew time, arrival time and required arrival time) is represented as a function of global sources of variation (denoted by X_i) and independent random sources of variation (denoted by S_i) in a canonical first-order (denoted by CFO) form. The advantages of such a formulation are that it can capture many of the key correlations and can produce delay sensitivities due to changes in a variety of environmental and process-related parameters [2]. Sources of variations have often been assumed to be Gaussian, which in turn simplifies the block-based σTA. However, it has been recently reported that certain process parameters exhibit non-Gaussian probability distributions [3].

Block-based σTA breaks its analysis into two parts: 1) variational interconnect timing analysis, and 2) variational gate timing analysis. Variational interconnect timing analysis has been studied by a

number of researchers. References [4] and [5] presented reduced order modeling approaches for interconnect propagation delay calculation, which accounts for manufacturing variations. These approaches are computationally expensive due to the lack of closed form expressions. The authors of [6] expressed the canonical first-order model of the interconnect delay in closed form and showed how to propagate it through the interconnect. The authors of [7] described a modeling technique for gate delay variability considering multiple input switching. In [8], a model for calculating statistical gate delay variations caused by intra-chip and inter-chip variabilities was presented. These works, however, do not provide an accurate means of analyzing the gate propagation delay and output slew time as a function of variational *RC*-π loads, statistical input transitions, and a variation-aware gate library. In this paper, two new techniques are presented for determining the variational gate timing behavior.

The first technique, called VGTA (for Variational Gate Timing Analysis), performs the following steps. Given the variational resistive-capacitive load (where all resistances and capacitances are represented in the CFO form), an efficient and accurate algorithm will be presented to calculate the variational *RC*-π load. To perform the analysis, we calculate the variation-aware admittance moments (cf. section 0), and as a result, the resistance and capacitances in the *RC*-π load can be written in the CFO form. Based on the statistical RC-π load obtained in this way, we calculate the variational effective capacitance in the CFO form. To accomplish this goal, first a new approach for effective capacitance calculation in static timing analysis (STA) is presented (cf. section 4.1.) This effective capacitance calculation method is used to calculate the variational effective capacitance considering non-Gaussian process and environmental sources of variation in the CFO form (cf. section 4.2.) Given statistical input transition times, variation-aware gate library, and variational effective capacitance (c_{eff}) load in the CFO form, we calculate variational gate delay and output transition time in the CFO form (cf. sections 2.2.1.)

The second technique, which is called F-VGTA for Fast Variational Gate Timing Analysis works as follows. The first step of F-VGTA is similar to the first step of VGTA algorithm. To determine the variational gate delay and output slew time in the CFO form, a “variation-aware effective

capacitance" technique is proposed in section 4.3, which is based on the single-iteration C_{eff} calculation approach of section 4.1.

We point out that although, in this paper, we focus on the random variables in CFO form to represent process and environmental sources of variation as well as the performance quantities of interest, the work itself is not limited to the first-order approximation of these sources of variation. In fact, it is straightforward to extend the approach to more complex (e.g., second-order) forms for both Gaussian and non-Gaussian parameter variations.

The remainder of this paper is organized as follows. In section 2, we review the background of parameterized block-based σTA. We also show how to convert a quantity, which itself is a function of global and independent sources of variation, into a canonical first-order (CFO) form. The variation-aware *RC*-π calculation is presented in section 0. Section 4 explains two new statistical gate timing analysis techniques which handle statistical input rise times, variation-aware gate library, and variational *RC*-π load. Section 5 presents experimental results. Finally, conclusions are discussed in section 6. We use the notation shown in Table 1 throughout the paper.

Table 1: Useful notation and terminology

Notation	Description
A	A deterministic variable (which does not take into account any statistical variation)
$\overset{\wp}{A}$	An arbitrary (non-CFO) random variable, which is a function of *m* global and *p* independent random sources of variation
$\overset{\triangleleft\triangleright}{A}$	A CFO random variable, which is a function of *m* global and *p* independent random sources of variation i.e., $\overset{\triangleleft\triangleright}{A} = A_0 + \sum_{i=1}^{m} A_i \Delta X_i + \sum_{k=1}^{p} A_{m+j} \Delta S_j$

2. Background

In σTA, it is required to evaluate the distribution of the delay and slew time of the critical paths. Until now, this goal has typically been achieved by calculating the mean and variance of the distributions of the delay and slew time. However, as mentioned earlier, sources of variation may have an arbitrary (i.e., non-Gaussian) distribution. Therefore, in general, in addition to calculating the mean and variance of the electrical and timing parameters, one must calculate at least the skewness of their distributions, i.e. one must at the minimum calculate the first three moments of the circuit parameter variations.

***Definition* 1**: The degree of asymmetry of a probability distribution function is called its skewness (denoted by κ.) A distribution, or data set, is symmetric if it looks the same to the left and right of the center point. The skewness of a normal distribution is zero. Negative values for the skewness indicate distributions which are skewed to the left whereas positive values for the skewness indicate distributions which are skewed to the right. By left (right) skew, we mean that the left (right) tail is heavier than the right (left) tail. The *skewness* of a distribution is defined to be $\kappa = \frac{\mu_3}{\sigma^3}$ where μ_3 is the 3rd central moment and σ^2 is the variance (second central moment.)

***Definition* 2:** We say X is equal to Y in the first three moments ($X \overset{d_3}{=} Y$) if the mean, variance, and skewness of X and Y are equal. (i.e., they have the same first three central moments.)

***Lemma* 1:** Suppose $\Delta S_1,\ldots,\Delta S_n$ are n independent random variables with distribution $\Delta S_i \sim Dist_i$ ($\mu=0$, $\sigma^2=1$, κ_i). Then,

$$\sum_{i=1}^{n} a_i \Delta S_i \overset{d_3}{=} \sqrt{\sum_{i=1}^{n} a_i^{\,2}} \cdot \Delta S_{eq} \quad \text{where} \quad \Delta S_{eq} \sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa = \frac{\sum_{i=1}^{n} a_i^{\,3} \cdot \kappa_i}{\left(\sqrt{\sum_{i=1}^{n} a_i^{\,2}} \right)^3} \right)$$

***Proof*:** Using expectation value properties, we have

$$E\left(\sum_{i=1}^{n} a_i \Delta S_i\right) = \sum_{i=1}^{n} E\left(a_i \Delta S_i\right) = \sum_{i=1}^{n} a_i E\left(\Delta S_i\right) = \sum_{i=1}^{n} a_i \cdot 0 = 0$$

and

$$E\left(\sqrt{\sum_{i=1}^{n} a_i^{\,2}} \cdot \Delta S_{eq}\right) = \sqrt{\sum_{i=1}^{n} a_i^{\,2}} \cdot E\left(\Delta S_{eq}\right)$$

From Definition 2, because the mean value of the two side of the equality should be equal

$$\sqrt{\sum_{i=1}^{n} a_i^{\,2}}\, E\left(\Delta S_{eq}\right) = 0 \quad \Rightarrow \quad E\left(\Delta S_{eq}\right) = 0$$

For the variance of ΔS_{eq}, we have

$$E\left(\sum_{i=1}^{n} a_i \Delta S_i\right)^2 = \sum_{i=1}^{n} E\left(a_i \Delta S_i\right)^2 + 2\sum_{i=1}^{n} \sum_{j=1 \neq i}^{n} E\left(a_i \Delta S_i \cdot a_j \Delta S_j\right)$$

Since ΔSi's are independent, we have

$$= \sum_{i=1}^{n} E\left(a_i \Delta S_i\right)^2 + 0 = \sum_{i=1}^{n} a_i^{\,2} E\left(\Delta S_i\right)^2 = \sum_{i=1}^{n} a_i^{\,2}$$

and

$$E\left(\sqrt{\sum_{i=1}^{n} a_i^{\,2}} \cdot \Delta S_{eq}\right)^2 = \sum_{i=1}^{n} a_i^{\,2} \cdot E\left(\Delta S_{eq}\right)^2$$

From Definition 2 and since the mean value of ΔS_{eq} is 0, then

$$\sum_{i=1}^{n} a_i^{\,2} E\left(\Delta S_{eq}\right)^2 = \sum_{i=1}^{n} a_i^{\,2} \quad \Rightarrow \quad E\left(\Delta S_{eq}\right)^2 = 0$$

$$\text{Since } E\left(\Delta S_{eq}\right) = 0 \quad \Rightarrow \quad \sigma_{\Delta S_{eq}}{}^2 = 1$$

In addition, for the skewness of ΔS_{eq} distribution, we have

$$E\left(\sum_{i=1}^{n} a_i \Delta S_i\right)^3 = \sum_{i=1}^{n} E\left(a_i \Delta S_i\right)^3 + 3\sum_{i=1}^{n}\sum_{j=1\neq i}^{n} E\left(\left(a_i \Delta S_i\right)^2 \cdot a_j \Delta S_j\right)$$

Since ΔS_i's are independent, we have

$$= \sum_{i=1}^{n} E\left(a_i \Delta S_i\right)^3 + 0 = \sum_{i=1}^{n} a_i{}^3 E\left(\Delta S_i\right)^3 = \sum_{i=1}^{n} a_i{}^3 \kappa_i$$

and

$$E\left(\sqrt{\sum_{i=1}^{n} a_i{}^2} \cdot \Delta S_{eq}\right)^3 = \left(\sqrt{\sum_{i=1}^{n} a_i{}^2}\right)^3 \cdot E\left(\Delta S_{eq}\right)^3$$

From Definitions 1 and 2

$$\left(\sqrt{\sum_{i=1}^{n} a_i{}^2}\right)^3 E\left(\Delta S_{eq}\right)^3 = \sum_{i=1}^{n} a_i{}^3 \kappa_i \quad \Rightarrow \quad E\left(\Delta S_{eq}\right)^3 = \frac{\sum_{i=1}^{n} a_i{}^3 \kappa_i}{\left(\sqrt{\sum_{i=1}^{n} a_i{}^2}\right)^3}$$

$$\text{Since } E\left(\Delta S_{eq}\right) = 0 \text{ and } \sigma_{\Delta S_{eq}}{}^2 = 1 \Rightarrow \quad \kappa_{\Delta S_{eq}} = \frac{\sum_{i=1}^{n} a_i{}^3 \kappa_i}{\left(\sqrt{\sum_{i=1}^{n} a_i{}^2}\right)^3}$$

■

2.1 Canonical First-Order (CFO) Representation for Timing and Electrical Parameter Modeling

In block-based statistical timing analysis tool, a first-order variational model is employed for all timing quantities such as the gate and wire delays, arrival times, required arrival times, slacks and slew times, i.e., any timing quantity, *a*, is expressed in the CFO form as:

$$\overset{\triangleleft\triangleright}{a} = a_0 + \sum_{i=1}^{m} a_i \Delta X_i + a_{m+1} \Delta S_a$$

where a_0 is the nominal value of the timing quantity of interest; ΔX_i's represent the variation of m global sources of variation, X_i, from their nominal values, a_i's are the sensitivities to each of the global sources of variation, ΔS_a is the variation of independent random variable S_a, and a_{m+1} is the sensitivity of the timing quantity to S_a. By scaling the sensitivity coefficients, we can assume that ΔX_i and ΔS_a have distributions with $\mu=0$ and $\sigma^2=1$ and skewness= κ denoted by $Dist(\mu=0,\sigma^2=1,\kappa)$. Moreover, we define a_i/a_0 as the *normalized sensitivity coefficient* (denoted by NSC.)

Variation in the physical dimensions of the wire causes change in its resistance and capacitance, thereby, making the gate delay and slew time as well as interconnect propagation delay and slew time to vary accordingly [9]. Therefore, we need to capture the effect of geometric variations on the electrical parameters of the interconnect. For instance, resistance and capacitance in the CFO form are calculated as follows:

$$\overset{\triangleleft\triangleright}{r} = r_0 + \sum_{i=1}^{m} r_i \Delta X_i + r_{m+1} \Delta S_r \qquad \overset{\triangleleft\triangleright}{c} = c_0 + \sum_{i=1}^{m} c_i \Delta X_i + c_{m+1} \Delta S_c$$

where r_0 and c_0 represent nominal resistance and capacitance values, computed when the wire dimensions are at their nominal (or typical) values. ΔX_i's are the global sources of variation and ΔS_r and ΔS_c represent the independent random sources of variation for the resistance and capacitance, respectively r_i and c_i are the sensitivity coefficients of resistance and capacitance with respect to the sources of variations, respectively. Again we have the assumption for the distribution of ΔX_i, ΔS_r, and ΔS_c.

***Observation*:** *Invariant Functional Form Property*: This property states that: $y = f(x) \Leftrightarrow \overset{\wp}{Y} = f(\overset{\wp}{X})$, which simply underlies the fact that the form of function f operating on some input variable x to

produce output variable y is independent of its input/output type (i.e., whether x and y are deterministic or variational.)

2.2 Converting a Variational Function into a CFO Form

As mentioned before, it is important to represent timing and electrical quantities in the CFO form. This in turn enables one to propagate first order sensitivities to different sources of variation through a timing graph [2][9]. Additionally, it makes variational computations efficient and practical and provides timing diagnostics at a very small cost in terms of the cpu time. The remaining question is how to convert a quantity of interest (which itself is a function of different CFO variables) into the CFO form.

The following subsection presents a technique to answer the above question. We use an important example to illustrate the various steps of the proposed procedure. The problem we address is how to convert the gate output transition time into the CFO form. However, this method can be easily applied to any other quantity of interest.

2.2.1 Example: Gate timing analysis for lumped capacitive load in block-based σTA

Problem Statement I: Given is a variational CMOS driver where its input rise time, t_{in}, is in the CFO form and drives an output capacitive load, also, in the CFO form. Note that the distribution characteristics of all global and independent sources of variation (μ=0, σ^2=1, κ) are given. The objective is to calculate the output transition time, t_r, in the CFO form:

$$\overset{\triangleleft\triangleright}{t}_r = t_{r,0} + \sum_{i=1}^{m} t_{r,i}\Delta X_i + t_{r,m+1}\Delta S_{t_r}$$

i.e., calculate the nominal value ($t_{r,0}$) and the sensitivity coefficients ($t_{r,i}$ and $t_{r,m+1}$) as well as the skewness of distribution of ΔS_{tr}.

The gate output transition time is a function of the input transition time, the logic gate characteristics (e.g., the W/L ratio, threshold voltage of transistors, V_{dd}, and temperature), and the

output load. In commercial ASIC cell libraries, it is possible to characterize various output transition times (e.g. 10%, 50%, and 90%) as a function of above variables; i.e.;

$$t_r = TF\left(t_{in}, c_l, z\right) \quad \text{where} \quad z = \left\{\frac{W}{L}, V_T, V_{dd}, Temp, \ldots\right\} \qquad (1)$$

where t_r is the output transition time and TF is the corresponding output transition time function. z captures the gate characteristics and environmental factors, t_{in} is the input transition time, and c_l is the output capacitive load. Based on the Invariant Functional Form Property, the form of function TF is independent of its input type (deterministic or variational.) Hence, we extend the above equation to the variational case. In block-based σTA, t_{in}, c_l, and every parameter z is given in the CFO form as a function of m global and exactly one independent random sources of variations. Therefore, t_r itself is a non-CFO random variable. Hence, to represent the non-CFO t_r in the CFO form, we replace t_{in}, c_l, and z with their corresponding CFO models and collect terms. Now, by differentiating with respect to the global and independent random sources of variation, t_r as a function of m global sources of variation and p independent random sources of variation can be approximated as:

$$\overset{\wp}{t}_r = TF\left(\Delta X_1 \ldots \Delta X_m, \Delta S_1 \ldots \Delta S_p\right) \Rightarrow$$

$$\overset{\wp}{t}_r \cong TF\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} + \sum_{i=1}^{m} \left.\frac{\partial TF}{\partial \Delta X_i}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \cdot \Delta X_i + \sum_{j=1}^{p} \left.\frac{\partial TF}{\partial \Delta S_j}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \cdot \Delta S_j \quad \text{where} \quad \begin{cases} l = 1 \ldots m \\ k = 1 \ldots p \end{cases} \qquad (2)$$

Considering that ΔS_j's are $Dist_j(\mu=0, \sigma^2=1, \kappa_j)$, Eqn.(2) can be re-written as:

$$\overset{\triangleleft\triangleright}{t}_r = TF\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} + \sum_{i=1}^{m} \left.\frac{\partial TF}{\partial \Delta X_i}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \cdot \Delta X_i + \sqrt{\sum_{j=1}^{p} \left(\left.\frac{\partial TF}{\partial \Delta S_j}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \right)^2} \cdot \Delta S_{t_r}$$

From Lemma 1,

$$\Delta S_{t_r} \sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa = \frac{\sum_{j=1}^{p}\left(\left.\frac{\partial TF}{\partial \Delta S_j}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}\right)^3 .\kappa_j}{\left(\sqrt{\sum_{j=1}^{p}\left(\left.\frac{\partial TF}{\partial \Delta S_j}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}\right)^2}\right)^3}\right)$$

In Lemma 2, we present the key results, which enable us to do addition, multiplication, and division of two CFO forms and putting the result in a new CFO form. (Notice that this lemma allows us to evaluate the above equation.)

Lemma* 2*: Suppose *a* and *b* are two given CFO random variables as follows:

$$\overset{\triangleleft\triangleright}{a} = a_0 + \sum_{i=1}^{m} a_i \Delta X_i + a_{m+1}\Delta S_a \qquad \overset{\triangleleft\triangleright}{b} = b_0 + \sum_{i=1}^{m} b_i \Delta X_i + b_{m+1}\Delta S_b$$

The following describes the result of various operations performed on *a* and *b*.

a) Addition and subtraction:

$$\overset{\triangleleft\triangleright}{c} = \overset{\triangleleft\triangleright}{a} \pm \overset{\triangleleft\triangleright}{b} = (a_0 \pm b_0) + \sum_{i=1}^{m} (a_i \pm b_i)\Delta X_i + \sqrt{{a_{m+1}}^2 + {b_{m+1}}^2}\,\Delta S_c$$

b) Multiplication:

$$\overset{\triangleleft\triangleright}{c} \cong \overset{\triangleleft\triangleright}{a} \times \overset{\triangleleft\triangleright}{b} = a_0 b_0 + \sum_{i=1}^{m} (a_0 b_i + a_i b_0)\Delta X_i + \sqrt{(a_0 b_{m+1})^2 + (a_{m+1} b_0)^2}\,\Delta S_c$$

c) Division:

$$\overset{\triangleleft\triangleright}{c} \cong \frac{\overset{\triangleleft\triangleright}{a}}{\overset{\triangleleft\triangleright}{b}} = \frac{a_0}{b_0} + \sum_{i=1}^{m} \frac{a_i b_0 - a_0 b_i}{{b_0}^2}\Delta X_i + \sqrt{\left(\frac{a_{m+1}}{b_0}\right)^2 + \left(\frac{a_0 b_{m+1}}{{b_0}^2}\right)^2}\,\Delta S_c$$

Proof: Based on the aforesaid operations, we have

$$\overset{\lhd\rhd}{c} = \left(\overset{\lhd\rhd}{a} \pm \overset{\lhd\rhd}{b}\right)\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m} \left.\frac{\partial\left(\overset{\lhd\rhd}{a} \pm \overset{\lhd\rhd}{b}\right)}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i + \sqrt{\sum_{j=1}^{2}\left(\left.\frac{\partial\left(\overset{\lhd\rhd}{a} \pm \overset{\lhd\rhd}{b}\right)}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2} \cdot \Delta S_c$$

$$= \overset{\lhd\rhd}{a}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \pm \overset{\lhd\rhd}{b}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m} \left.\frac{\partial \overset{\lhd\rhd}{a}}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i \pm \sum_{i=1}^{m} \left.\frac{\partial \overset{\lhd\rhd}{b}}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i + \sqrt{\sum_{j=1}^{2}\left(\left.\frac{\partial \overset{\lhd\rhd}{a}}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2 + \sum_{j=1}^{2}\left(\left.\frac{\partial \overset{\lhd\rhd}{b}}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2} \cdot \Delta S_c$$

$$= a_0 \pm b_0 + \sum_{i=1}^{m} a_i \Delta X_i + \sum_{i=1}^{m} b_i \Delta X_i + \sqrt{{a_{m+1}}^2 + {b_{m+1}}^2}\,\Delta S_c$$

which proves part (a). For part (b), we have

$$\overset{\lhd\rhd}{c} = \left(\overset{\lhd\rhd}{a} \times \overset{\lhd\rhd}{b}\right)\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m} \left.\frac{\partial\left(\overset{\lhd\rhd}{a} \times \overset{\lhd\rhd}{b}\right)}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i + \sqrt{\sum_{j=1}^{2}\left(\left.\frac{\partial\left(\overset{\lhd\rhd}{a} \times \overset{\lhd\rhd}{b}\right)}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2} \cdot \Delta S_c$$

$$= \overset{\lhd\rhd}{a}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \times \overset{\lhd\rhd}{b}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m} \left.\frac{\partial \overset{\lhd\rhd}{a}}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \overset{\lhd\rhd}{b}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i + \sum_{i=1}^{m} \overset{\lhd\rhd}{a}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \left.\frac{\partial \overset{\lhd\rhd}{b}}{\partial \Delta X_i}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \Delta X_i$$

$$+ \sqrt{\sum_{j=1}^{2}\left(\left.\frac{\partial \overset{\lhd\rhd}{a}}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \overset{\lhd\rhd}{b}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2 + \sum_{j=1}^{2}\left(\overset{\lhd\rhd}{a}\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} \cdot \left.\frac{\partial \overset{\lhd\rhd}{b}}{\partial \Delta S_j}\right|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2} \cdot \Delta S_c$$

$$= a_0 \times b_0 + \sum_{i=1}^{m} a_i b_0 \Delta X_i + \sum_{i=1}^{m} a_0 b_i \Delta X_i + \sqrt{{a_{m+1}}^2 {b_0}^2 + {a_0}^2 {b_{m+1}}^2}\,\Delta S_c$$

Part (c) can be proved similarly. Therefore, we can write

$$\overset{\triangleleft\triangleright}{c} \cong \frac{\overset{\triangleleft\triangleright}{a}}{\overset{\triangleleft\triangleright}{b}} = \frac{a_0}{b_0} + \sum_{i=1}^{m} \frac{a_i b_0 - a_0 b_i}{{b_0}^2} \cdot \Delta X_i + \sqrt{\left(\frac{a_{m+1}}{b_0}\right)^2 + \left(\frac{a_0 b_{m+1}}{{b_0}^2}\right)^2} \cdot \Delta S_c$$

$$\overset{\triangleleft\triangleright}{c} = \left.\frac{\overset{\triangleleft\triangleright}{a}}{\overset{\triangleleft\triangleright}{b}}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} + \sum_{i=1}^{m} \left.\frac{\partial\left(\frac{\overset{\triangleleft\triangleright}{a}}{\overset{\triangleleft\triangleright}{b}}\right)}{\partial \Delta X_i}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \cdot \Delta X_i + \sqrt{\sum_{j=1}^{2} \left(\left.\frac{\partial\left(\frac{\overset{\triangleleft\triangleright}{a}}{\overset{\triangleleft\triangleright}{b}}\right)}{\partial \Delta S_j}\right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \right)^2} \cdot \Delta S_c$$

$$= \frac{a_0}{b_0} + \sum_{i=1}^{m} \frac{a_i b_0 - a_0 b_i}{{b_0}^2} \cdot \Delta X_i + \sqrt{\left(\frac{a_{m+1}}{b_0}\right)^2 + \left(\frac{a_0 b_{m+1}}{{b_0}^2}\right)^2} \cdot \Delta S_c$$

■

3. RC-π Load Calculation in the CFO Form

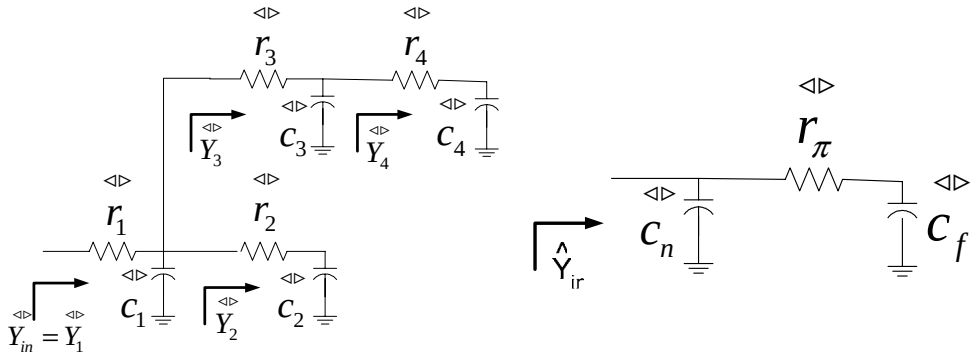
In VDSM technologies, one cannot neglect the effect of interconnect resistance of the load on the gate delay and output transition time. In STA, an adequate approximation of an n^{th} order load seen by the gate (i.e., a load with n distributed capacitances to ground) is obtained by replacing the load by a second order *RC*-π model [10]. Equating the first, second, and third moments of the admittance of the real load with the first, second, and third moments of the *RC*-π load, we can compute c_n, r_π, and c_f as follows [11]:

$$c_n = Y_{1,in} - \frac{{Y_{2,in}}^2}{Y_{3,in}} \qquad r_\pi = -\frac{{Y_{3,in}}^2}{{Y_{2,in}}^3} \qquad c_f = \frac{{Y_{2,in}}^2}{Y_{3,in}} \qquad (3)$$

where $Y_{k,in}$ denotes the k^{th} moment of the admittance of the real load. In σTA, it is necessary to consider the effect of variability of the load on the gate timing analysis.

Problem Statement II: Given is an *RC* network representation of the load of a logic gate in a design as exemplified in Figure 1(a), where each *r* and *c* is in the CFO form. Note that the distribution characteristics of all global and independent sources of variation ($\mu=0$, $\sigma^2=1$, κ) are given. The

objective is to calculate an equivalent variational *RC*-π load (where c_n, r_π, and c_f are in the CFO form), while its admittance matches the admittance of the real load in the frequency range of interest.



(a) (b)

Figure 1: (a) a variational *RC* network representation of a net in a design. (b) the equivalent variational *RC*-π model.

c_n, r_π, and c_f are functions of the admittance moments as seen from Eqn. (3). Hence, by calculating the variational admittance moments, we can calculate the CFO parameters of the *RC*-π load (by using the equations given in section 2.2.) This can be done by differentiating expressions in Eqn. (3) with respect to the sources of variation (c.f. section 2.2.) However, as it will be shown next, a recursive operation is utilized to calculate the variational admittance moments. In each recursion step returns a non-CFO random variable which will feed in the next recursion step and this may increase the complexity of the calculations.

Therefore, instead, we represent the admittance moments in the CFO form throughout the recursion. This helps us by controlling the complexity of representing the moments as the recursive function proceeds. The following shows how to calculate the input admittance moments of a real load in the CFO form.

Consider the *RCY* segment shown in Figure 2. Assume that the admittances at nodes *j* and *i* are represented by infinite series using the admittance moments:

$$Y_j(s) = sY_{1,j} + s^2Y_{2,j} + ... + s^kY_{k,j} + ...$$

$$Y_i(s) = sY_{1,i} + s^2Y_{2,i} + ... + s^kY_{k,i} + ...$$

where $Y_{k,j}$ denotes the k^{th} moment of the admittance of the node j. In STA, the admittance at node i is recursively computed in terms of the admittance at node j as follows [11]:

$$\begin{aligned} Y_{1,i} &= Y_{1,j} + c_i \\ Y_{k,i} &= Y_{k,j} - r_i \sum_{l=1}^{k-1} Y_{l,i} Y_{k-l,j} - r_i c_i Y_{k-1,i} \quad for \;\; k \geq 2 \end{aligned} \tag{4}$$

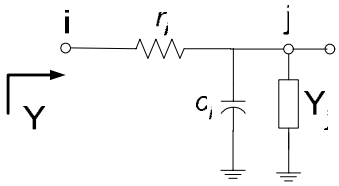


Figure 2: an *RCY* segment model for recursive admittance moment calculation.

Using the Invariant Functional Form Property, we extend the above equation to the variational case. Assume the admittance moments of node j are written in the CFO form. Thus, by differentiating $Y_{k,i}$ with respect to the sources of variations, the $Y_{k,i}$ moments can be also represented in the CFO form (c.f. section 2.2.)

As an example, consider the circuit shown in Figure 1. To calculate the admittance moments of Y_{in}=Y_1 in the CFO form, we need to start from the far end nodes of the *RC* tree (Y_2 and Y_4) and recursively apply Eqn. (4). Therefore, we calculate the first three moments of Y_4 in the CFO form as follows:

1) $\overset{\triangleleft\triangleright}{Y}_{1,4} = \overset{\triangleleft\triangleright}{c}_4$;

2) $\overset{\wp}{Y}_{2,4} = -\overset{\triangleleft\triangleright}{r}_4 \overset{\triangleleft\triangleright}{c}_4 \overset{\triangleleft\triangleright}{Y}_{1,4} = -\overset{\triangleleft\triangleright}{r}_4 \overset{\triangleleft\triangleright}{c}_4^{\,2}$;

3) Calculate $\overset{\triangleleft\triangleright}{Y}_{2,4}$;

4) $\overset{\wp}{Y}_{3,4} = -\overset{\triangleleft\triangleright}{r}_4 \overset{\triangleleft\triangleright}{c}_4 \overset{\triangleleft\triangleright}{Y}_{2,4}$;

5) Calculate $\overset{\triangleleft\triangleright}{Y}_{3,4}$;

Based on the problem statement assumption, c_4 is in the CFO form, thereby, $Y_{1,4}$ is also in the CFO form. However, since $Y_{2,4}$ and $Y_{3,4}$ are nonlinear functions of the CFO variables and as a result they are complex random variables, we ought to use the techniques described in section 2.2 to transform $Y_{2,4}$ and $Y_{3,4}$ to the CFO form. Similarly, the first three admittance moments of Y_3 as a function of the moments of Y_4 are obtained as:

1) $\overset{\triangleleft\triangleright}{Y}_{1,3} = \overset{\triangleleft\triangleright}{Y}_{1,4} + \overset{\triangleleft\triangleright}{c}_3 = \overset{\triangleleft\triangleright}{c}_4 + \overset{\triangleleft\triangleright}{c}_3$;

2) $\overset{\wp}{Y}_{2,3} = \overset{\triangleleft\triangleright}{Y}_{2,4} - \overset{\triangleleft\triangleright}{r}_3 \overset{\triangleleft\triangleright}{Y}_{1,3} \overset{\triangleleft\triangleright}{Y}_{1,4} - \overset{\triangleleft\triangleright}{r}_3 \overset{\triangleleft\triangleright}{c}_3 \overset{\triangleleft\triangleright}{Y}_{1,3}$;

3) Calculate $\overset{\triangleleft\triangleright}{Y}_{2,3}$;

4) $\overset{\wp}{Y}_{3,3} = \overset{\triangleleft\triangleright}{Y}_{3,4} - \overset{\triangleleft\triangleright}{r}_3 \left(\overset{\triangleleft\triangleright}{Y}_{1,3} \overset{\triangleleft\triangleright}{Y}_{2,4} + \overset{\triangleleft\triangleright}{Y}_{2,3} \overset{\triangleleft\triangleright}{Y}_{1,4} \right) - \overset{\triangleleft\triangleright}{r}_3 \overset{\triangleleft\triangleright}{c}_3 \overset{\triangleleft\triangleright}{Y}_{2,3}$;

5) Calculate $\overset{\triangleleft\triangleright}{Y}_{3,3}$;

By using the above recursive operations, we easily compute the moments of Y_{in}=Y_1 in the CFO form, and hence, calculate the values of c_n, r_π, and c_f in the CFO form using Eqn. (3).

4. Gate Timing Analysis for the RC-π Load in Block-Based σTA

Problem statement III: Given is a variational CMOS driver, whose input rise time, t_{in}, is in the CFO form and drives a variational *RC*-π load. The resistance and two capacitances of this load are also in the CFO forms. Note that the distribution characteristics of all global and independent sources

of variation (μ=0, σ^2=1, κ) are given. The objective is to calculate the output transition time, t_r, in the CFO form:

$$\overset{\triangleleft\triangleright}{t_r} = t_{r,0} + \sum_{i=1}^{m} t_{r,i}\Delta X_i + t_{r,m+1}\Delta S_{t_r}$$

i.e., calculate the nominal value ($t_{r,0}$) and the sensitivity coefficients ($t_{r,i}$ and $t_{r,m+1}$) as well as the skewness of distribution of ΔS_{tr}.

Section 2.2.1 solves the same problem where the gate drives a variational purely-capacitive load in the CFO form. (cf. Eqn. (1)) Therefore, if we substitute the *RC*-π load with its equivalent variational effective capacitance, c_{eff}, in the CFO form, then the solution to problem statement I is an acceptable solution to problem statement III. Based on this reasoning, the following subsections propose a solution for calculating the effective capacitance in the CFO form. Section 4.1 presents a new effective capacitance calculation method in static timing analysis. This method is used in section 4.2 where a technique for statistical effective capacitance calculation is presented. Section 4.3 utilizes a heuristic combined with the technique presented in section 4.1 to present the second technique for faster variational gate timing analysis in section 4.3.

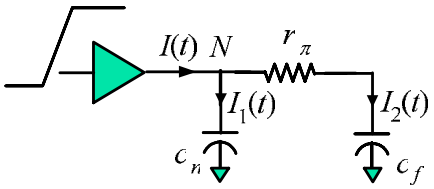
4.1 A New Effective Capacitance Calculation Method in STA

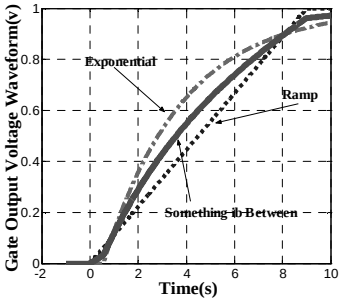
The effective capacitance is a pure capacitance that replaces an *RC*-π load and has the property that it gives the most accurate result from a timing model that is characterized with lumped capacitance. Typically, the effective capacitance stores the same amount of charge as the *RC*-π load until a certain point of the output voltage transition [11][12][13] (e.g., the 50% trip point of the output transition.) Figure 3(a) depicts a typical CMOS driver with its input waveform and *RC*-π load. The output voltage waveform may be modeled as a weighted linear sum of ramp and exponential waveforms as shown in Figure 3(b). We therefore assume that the *actual* c_{eff} can be obtained as a weighted average of that obtained for the ramp output waveform and that obtained for the exponential output waveform.

In the following, we calculate c_{eff} for ramp and exponential waveforms of the gate output voltage. Suppose that output voltage of a gate is approximated with an exponential waveform:

$$V_N(t) = V_{dd}\left(1 - e^{-pt}\right) \quad \text{where} \quad p = \frac{\ln\left(\frac{1-\alpha}{1-\beta}\right)}{t_r}$$

where $V_N(t)$ is the gate output voltage waveform in time domain and t_r is the output rise time from α% trip point to β% trip point of this waveform.





(a) (b)

Figure 3: (a) A gate, which drives an *RC*- π calculated load. (b) Gate output waveform is neither ramp nor exponential.

t_r is a function of the input transition time (t_{in}) and the output load. Thus, the iterative effective capacitance equation for matching any θ% trip point of the gate output transition time may be written as:

$$c_{eff}^{Exp}(\theta) = G\left(t_r, c_n, r_\pi, c_f\right) = c_n + k_{Exp}(\theta)\, c_f \quad \text{where}$$

$$k_{Exp}(\theta) = \left[1 + \frac{y}{\theta}\left(e^{\ln(1-\theta)/y} - 1\right)\right] \quad \text{and}$$

$$y = \ln\left(\frac{1-\alpha}{1-\beta}\right) \cdot \frac{r_\pi c_f}{t_r\left(t_{in}, c_{eff}^{\ Exp}(\theta)\right)}$$

Similarly, for the ramp output voltage waveform, we have:

$$c_{eff}^{Ramp}(\theta) = H\left(t_r, c_n, r_\pi, c_f\right) = c_n + k_{Ramp}(\theta)\cdot c_f \quad \text{where}$$

$$k_{Ramp}(\theta) = \left[1 - \frac{x}{\theta}\cdot\left(1 - \mathrm{e}^{-\theta/x}\right)\right] \quad \text{and}$$

$$x = (\beta - \alpha)\cdot\frac{r_\pi c_f}{t_r\left(t_{in}, c_{eff}^{\ Ramp}(\theta)\right)}$$

Now, based on the assumption made above, an iterative equation for actual c_{eff} calculation for any θ% trip point of the output transition may be written as:

$$\left.\begin{aligned} c_{eff}^{Exp}(\theta) &= G\left(t_r\left(t_{in}, c_{eff}^{Exp}(\theta)\right), c_n.r_\pi, c_f\right) \\ c_{eff}^{Ramp}(\theta) &= H\left(t_r\left(t_{in}, c_{eff}^{Ramp}(\theta)\right), c_n.r_\pi, c_f\right) \end{aligned}\right\} \Rightarrow$$

$$c_{eff}(\theta) = F\left(t_r\left(t_{in}, c_{eff}(\theta)\right), c_n.r_\pi, c_f\right) = \zeta\cdot G + (1-\zeta)\cdot H \qquad (5)$$

where $0 \le \zeta \le 1$ is the weighting factor for the linear combination of exponential and ramp waveforms. In practice, we have observed that when θ%=50%, then ζ=0.5 results in the minimum error between the iterative c_{eff} equation in Eqn. (5) and the actual sign-off c_{eff} value.

4.2 Variational Gate Timing Analysis (VGTA)

Suppose t_{in}, c_n, r_π, and c_f are given in the CFO form as:

$$\overset{\triangleleft\triangleright}{t_{in}} = t_{in,0} + \sum_{i=1}^{m} t_{in,i}\Delta X_i + t_{in,m+1}\Delta S_{t_{in}} \qquad (6)$$

$$\overset{\triangleleft\triangleright}{c_n} = c_{n,0} + \sum_{i=1}^{m} c_{n,i}\Delta X_i + c_{n,m+1}\Delta S_{c_n} \qquad (7)$$

$$\overset{\triangleleft\triangleright}{r_\pi} = r_{\pi,0} + \sum_{i=1}^{m} r_{\pi,i}\Delta X_i + r_{\pi,m+1}\Delta S_{r_\pi} \tag{8}$$

$$\overset{\triangleleft\triangleright}{c_f} = c_{f,0} + \sum_{i=1}^{m} c_{f,i}\Delta X_i + c_{f,m+1}\Delta S_{c_f} \tag{9}$$

$$\begin{aligned} \Delta S_{t_{in}} &\sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa_{t_{in}}\right) \qquad \Delta S_{c_n} \sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa_{c_n}\right) \\ \Delta S_{r_\pi} &\sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa_{r_\pi}\right) \qquad \Delta S_{c_f} \sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa_{c_f}\right) \end{aligned} \tag{10}$$

The effective capacitance for this problem generally becomes an arbitrary (non-CFO) random variable, i.e. $\overset{\wp}{c}_{eff}$. Thus, we approximate it with its CFO form and the objective becomes to calculate the coefficients of c_{eff} in the CFO form as well as the skewness of ΔS_{ceff} as:

$$\overset{\triangleleft\triangleright}{c_{eff}} = c_{eff,0} + \sum_{i=1}^{m} c_{eff,i}\Delta X_i + c_{eff,m+1}\Delta S_{c_{eff}} \tag{11}$$

such that $E\left[\left(\overset{\triangleleft\triangleright}{c_{eff}} - F\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, \overset{\triangleleft\triangleright}{c_{eff}}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right)\right)^2\right]$ is minimized.

Function F is given in Eqn. (5) and $E(.)$ denotes the expectation value.

***Theorem*:** For a variational circuit, where t_{in}, c_n, r_π, and c_f in the CFO form are written as in Eqns. (6)-(10), the coefficients of c_{eff} in the CFO form (Eqn. (11)), can be calculated as:

$$c_{eff,0} = F\left(t_r\left(t_{in,0}, c_{eff,0}\right), c_{n,0}, r_{\pi,0}, c_{f,0}\right) \tag{12}$$

$$c_{eff,i} = \frac{\left(\frac{\partial t_r}{\partial t_{in}}\right)^{nom} \cdot \left(\frac{\partial F}{\partial t_r}\right)^{nom} \cdot t_{in,i} + \left(\frac{\partial F}{\partial c_n}\right)^{nom} \cdot c_{n,i}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom} \cdot \left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}} + \frac{\left(\frac{\partial F}{\partial r_\pi}\right)^{nom} \cdot r_{\pi,i} + \left(\frac{\partial F}{\partial c_f}\right)^{nom} \cdot c_{f,i}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom} \cdot \left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}} \tag{13}$$

$$c_{eff,m+1} = \sqrt{\left(c_{eff,m+1}^{t_{in}}\right)^2 + \left(c_{eff,m+1}^{c_n}\right)^2 + \left(c_{eff,m+1}^{r_\pi}\right)^2 + \left(c_{eff,m+1}^{c_f}\right)^2} \tag{14}$$

$$\Delta S_{c_{eff}} \sim Dist\left(\mu = 0, \sigma^2 = 1, \kappa = \frac{\sum_{u \in U}\left(c_{eff,m+1}^{u}\right)^3 \kappa_u}{\left(\sum_{u \in U}\left(c_{eff,m+1}^{u}\right)^2\right)^{3/2}}\right) \tag{15}$$

where $U = \left\{'t_{in}', 'c_n', 'r_\pi', 'c_f'\right\}$

and

$$c_{eff,m+1}^{t_{in}} = \frac{\left(\frac{\partial F}{\partial t_r}\right)^{nom}\left(\frac{\partial t_r}{\partial t_{in}}\right)^{nom} \cdot t_{in,m+1}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom}\left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}} \qquad c_{eff,m+1}^{c_n} = \frac{\left(\frac{\partial F}{\partial c_n}\right)^{nom} \cdot c_{n,m+1}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom}\left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}}$$

$$c_{eff,m+1}^{r_\pi} = \frac{\left(\frac{\partial F}{\partial r_\pi}\right)^{nom} \cdot r_{\pi,m+1}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom}\left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}} \qquad c_{eff,m+1}^{c_f} = \frac{\left(\frac{\partial F}{\partial c_f}\right)^{nom} \cdot c_{f,m+1}}{1 - \left(\frac{\partial F}{\partial t_r}\right)^{nom}\left(\frac{\partial t_r}{\partial c_{eff}}\right)^{nom}}$$

***Proof*:** Based on the proposed effective capacitance equations in section 4.1, the c_{eff} iterative equation can be rewritten as:

$$c_{eff} = F\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, c_{eff}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right) = \zeta \cdot G\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, c_{eff}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right) + (1-\zeta) \cdot H\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, c_{eff}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right)$$

Next, we need to compute $\overset{\triangleleft\triangleright}{c_{eff}}$ such that:

$$E\left[\left(\overset{\triangleleft\triangleright}{c_{eff}} - F\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, \overset{\triangleleft\triangleright}{c_{eff}}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right)\right)^2\right] \text{ is minimized} \quad (16)$$

$$\begin{aligned}\overset{\triangleleft\triangleright}{c_{eff}} &= c_{eff,0} + \sum_{i=1}^{m} c_{eff,i}\Delta X_i + c_{eff,m+1}\Delta S_{c_{eff}} \\ &= c_{eff,0} + \sum_{i=1}^{m} c_{eff,i}\Delta X_i + c^{t_{in}}_{eff,m+1}\Delta S_{t_{in}} + c^{c_n}_{eff,m+1}\Delta S_{c_n} \\ &\quad + c^{r_\pi}_{eff,m+1}\Delta S_{r_\pi} + c^{c_f}_{eff,m+1}\Delta S_{c_f}\end{aligned}$$

Using the partial derivations technique, we can expand the non-linear function *F* around the global and independent sources of variation as:

$$\begin{aligned}F\left(t_r\left(\overset{\triangleleft\triangleright}{t_{in}}, \overset{\triangleleft\triangleright}{c_{eff}}\right), \overset{\triangleleft\triangleright}{c_n}, \overset{\triangleleft\triangleright}{r_\pi}, \overset{\triangleleft\triangleright}{c_f}\right) &\cong F\left(t_r\left(t_{in,0}, c_{eff,0}\right), c_{n,0}, r_{\pi,0}, c_{f,0}\right) \\ &+ \sum_{i=1}^{m} \frac{\partial}{\partial \Delta X_i} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \Delta X_i + \frac{\partial}{\partial \Delta S_{t_{in}}} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \Delta S_{t_{in}} + \frac{\partial}{\partial \Delta S_{c_n}} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \Delta S_{c_n} \\ &+ \frac{\partial}{\partial \Delta S_{r_\pi}} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \Delta S_{r_\pi} + \frac{\partial}{\partial \Delta S_{c_f}} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \Delta S_{c_f}\end{aligned}$$

Therefore, to satisfy Eqn. (16), we need to have:

$$c_{eff,0} = F\left(t_r\left(t_{in,0}, c_{eff,0}\right), c_{n,0}, r_{\pi,0}, c_{f,0}\right)$$

$$\begin{aligned} c_{eff,i} &= \frac{\partial}{\partial \Delta X_i} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \qquad \forall i \in \{1...m\} \\ \text{and} \quad c^U_{eff,m+1} &= \frac{\partial}{\partial \Delta S_U} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} \quad \text{for } U \in \left\{'t_{in}', 'c_n', 'r_\pi', 'c_f'\right\} \end{aligned} \tag{17}$$

Expanding Eqn. (17) will give us the following:

$$c_{eff,i} = \frac{\partial}{\partial \Delta X_i} F\Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}} = \left\{ \begin{aligned} &\frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial \overset{\lhd\rhd}{c_{eff}}} \cdot \frac{\partial \overset{\lhd\rhd}{c_{eff}}}{\partial \Delta X_i} + \frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial \overset{\lhd\rhd}{t_{in}}} \cdot \frac{\partial \overset{\lhd\rhd}{t_{in}}}{\partial \Delta X_i} + \\ &+ \frac{\partial F}{\partial \overset{\lhd\rhd}{c_n}} \cdot \frac{\partial \overset{\lhd\rhd}{c_n}}{\partial \Delta X_i} + \frac{\partial F}{\partial \overset{\lhd\rhd}{r_\pi}} \cdot \frac{\partial \overset{\lhd\rhd}{r_\pi}}{\partial \Delta X_i} + \frac{\partial F}{\partial \overset{\lhd\rhd}{c_f}} \cdot \frac{\partial \overset{\lhd\rhd}{c_f}}{\partial \Delta X_i} \end{aligned} \right|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}$$

$$= \left(\frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial c_{eff}} \cdot c_{eff,i} + \frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial t_{in}} \cdot t_{in,i} + \frac{\partial F}{\partial c_n} \cdot c_{n,i} + \frac{\partial F}{\partial r_\pi} \cdot r_{\pi,i} + \frac{\partial F}{\partial c_f} \cdot c_{f,i} \right) \Bigg|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}$$

Therefore, $c_{eff,i}$ value can be calculated as Eqn. (13). Using the same method, we can derive $c_{eff,m+1}^{\ tin}$.

$$c_{eff,m+1}^{t_{in}} = \frac{\partial}{\partial \Delta S_{t_{in}}} F \Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}$$

$$= \left(\frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial \overset{\triangleleft\triangleright}{c_{eff}}} \cdot \frac{\partial \overset{\triangleleft\triangleright}{c_{eff}}}{\partial \Delta S_{t_{in}}} + \frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial \overset{\triangleleft\triangleright}{t_{in}}} \cdot \frac{\partial \overset{\triangleleft\triangleright}{t_{in}}}{\partial \Delta S_{t_{in}}} \right) \Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}$$

$$= \left(\frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial c_{eff}} \cdot c_{eff,m+1}^{t_{in}} + \frac{\partial F}{\partial t_r} \cdot \frac{\partial t_r}{\partial t_{in}} \cdot c_{eff,m+1}^{t_{in}} \right) \Big|_{\substack{\Delta X_l = 0 \\ \Delta S_k = 0}}$$

where $c_{eff,m+1}^{t_{in}}$ will be calculated after collecting terms. Similarly $c_{eff,m+1}^{c_n}$, $c_{eff,m+1}^{r_\pi}$ and $c_{eff,m+1}^{c_f}$ are calculated and Eqn. (14) is proved. Finally Lemma 1 proves Eqn.(15).■

Eqn. (12) is the iterative c_{eff} calculation under the nominal conditions of the circuit. Hence, $c_{eff,0}$ can be evaluated by using the effective capacitance calculation presented in section 4.1 or any conventional effective capacitance calculation[12][13].

$t_{in,i}$, $c_{n,i}$, $r_{\pi,i}$, $c_{f,i}$, are given (cf. Eqns. (6)-(9).) To evaluate Eqns. (13) and (14), we must calculate the derivatives of function F (function F is given in Eqn. (5)) with respect to t_r, c_n, r_π, c_f, and evaluate these derivatives for the nominal values of the circuit parameters (when all sources of variation are set to zero i.e., $(\partial F/\partial t_r)^{nom}$, $(\partial F/\partial c_n)^{nom}$, $(\partial F/\partial r_\pi)^{nom}$, and $(\partial F/\partial c_f)^{nom}$.) These terms are easy to evaluate. For the remaining terms, we need to calculate the derivatives of the output transition time (t_r) with respect to t_{in} and c_{eff} and evaluate them under the nominal condition of the circuit (i.e., $(\partial t_r/\partial t_{in})^{nom}$ and $(\partial t_r/\partial c_{eff})^{nom}$.) To do this, we propose two different solutions.

1) **Updating the gate library look-up table and utilizing the additional data during σTA:** The revised tables now provide not only the timing quantity for each combination of t_{in} and c_l, but also the derivatives of the timing quantity (t_r) with respect to t_{in} and c_l for each combination of t_{in} and c_l.

2) **Using the existing gate library look-up table, but performing additional calculations during σTA:** To approximately calculate $(\partial t_r/\partial t_{in})^{nom}$, we read t_r (from the gate library) for $< t_{in,0} ; c_{l,0} >$ and $< t_{in,0}+\delta; c_{l,0} >$. Next, we calculate $\Delta t_r/\delta$ as the approximation. $(\partial t_r/\partial c_{eff})^{nom}$ can be similarly calculated.

Using any of the above solutions, Eqns. (13) and (14) become closed form expressions, which can be evaluated in constant time. Note that we calculate $(\partial F/\partial t_r)^{nom}$, $(\partial F/\partial c_n)^{nom}$, $(\partial F/\partial r_\pi)^{nom}$, and $(\partial F/\partial c_f)^{nom}$ only once in constant time. The complexity of our method is thus dominated by the iterative effective capacitance calculation under the nominal conditions. It is therefore important to try and improve the efficiency of the statistical c_{eff} calculation as is done in the next sections

4.3 Fast Variational Gate Timing Analysis (F-VGTA)

As mentioned earlier, to perform accurate gate delay and output slew time calculation, an iterative calculation of c_{eff} is inevitable [12][13]. However, as the number of sources of variations increases, the number of required c_{eff} runs rises exponentially (it is proportional to the number of corner points in static timing analysis), which becomes very CPU-intensive very quickly. In the previous section, we presented a statistical c_{eff} calculation technique. Here, we present another, more efficient, technique to find c_{eff} in the CFO form.

Suppose the actual c_{eff} in the CFO from can be represented as:

$$\overset{\triangleleft\triangleright}{c_{eff}} = c_{eff,0} + \sum_{i=1}^{m} c_{eff,i}\Delta X_i + c_{eff,m+1}\Delta S_{c_{eff}} = c_{eff,0}\left(1 + \sum_{i=1}^{m} \frac{c_{eff,i}}{c_{eff,0}}\Delta X_i + \frac{c_{eff,m+1}}{c_{eff,0}}\Delta S_{c_{eff}}\right) \quad (18)$$

Since c_{eff} calculation is iterative, we define $\overset{\triangleleft\triangleright}{c^k_{eff}}$ as an approximate representation of actual $\overset{\triangleleft\triangleright}{c_{eff}}$, which is obtained from the first k iterations of the statistical iterative c_{eff} algorithm as follows:

$$\overset{\triangleleft\triangleright}{c^k_{eff}} = c^k_{eff,0} + \sum_{i=1}^{m} c^k_{eff,i}\Delta X_i + c^k_{eff,m+1}\Delta S_{c^k_{eff}} = c^k_{eff,0}\left(1 + \sum_{i=1}^{m} \frac{c^k_{eff,i}}{c^k_{eff,0}}\Delta X_i + \frac{c^k_{eff,m+1}}{c^k_{eff,0}}\Delta S_{c^k_{eff}}\right) \quad (19)$$

c_{eff}^{0} means representing c_{eff} using the total capacitance (i.e. c_n+c_f), c_{eff}^{1} means the value of the effective capacitance obtained by using a single iteration, and so on. We define $c_{eff}^{k}{}_{,i}/c_{eff}^{k}{}_{,0}$ and $c_{eff,i}/c_{eff,0}$ as iterative and actual *normalized sensitivity coefficients* (denoted by NSC's), respectively. The NSC's capture the effect of the load variation on the c_{eff} value. It can be shown that in each iteration, the iterative NSC's change slightly (for $k \geq 1$), and they converge to their actual *NSC* values; i.e.;

$$\frac{c_{eff,i}}{c_{eff,0}} \cong \frac{c_{eff,i}^{k}}{c_{eff,0}^{k}} \qquad \begin{matrix} 1 \leq i \leq m, \\ 1 \leq k \end{matrix} \qquad (20)$$

Using the above observation, problem statement III can be solved by the following steps:

1) Evaluate $\overset{\triangleleft\triangleright}{c}_{eff}^{k}$ (section 4.1) and therefore find $c_{eff,0}^{k}$ and $c_{eff,i}^{k}$ for $1 \leq i \leq m+1$.

2) Find the actual $c_{eff,0}$ by performing conventional iterative effective capacitance algorithm for the nominal conditions of the circuit.

3) Using Eqn. (20) and the results of steps 1 and 2 , determine

$$c_{eff,i} = c_{eff,0} \cdot \frac{c_{eff,i}^{k}}{c_{eff,0}^{k}} \quad \forall i, 1 \leq i \leq m+1$$

4) Having found $c_{eff,0}$ and $c_{eff,i}$, for $1 \leq i \leq m+1$, calculate $\overset{\triangleleft\triangleright}{c}_{eff}$. Using the method presented in section 2.2, determine the gate delay and output slew in the CFO form and the skewness of ΔS_{t_α}.

Figure 4: (a) A gate, which drives an *RC*- π calculated load. (b) Gate output waveform is neither ramp nor exponential

Step 2 is performed by using STA-based (non-variational) C_{eff} algorithm presented in section 4.1 or any other conventional effective capacitance calculation [12][13]. Step 3 is a simple algebraic equation while step 4 is performed as per section 2.3. For step 1, the following sections show how to calculate the $\overset{\triangleleft\triangleright}{c}_{eff}^{0}$ and $\overset{\triangleleft\triangleright}{c}_{eff}^{1}$.

4.3.1 Finding $\overset{\triangleleft\triangleright}{c}_{eff}$ from $\overset{\triangleleft\triangleright}{c}^{0}_{eff}$

As we mentioned before, $c_{eff}^{\ 0}$ approximates c_{eff} with the sum of the total capacitance (i.e., c_n+c_f). Thus, the $\overset{\triangleleft\triangleright}{c}^{0}_{eff}$ is equal to the sum of $\overset{\triangleleft\triangleright}{c}_{n}$ and $\overset{\triangleleft\triangleright}{c}_{f}$, i.e. if

$$\overset{\triangleleft\triangleright}{c}_n = c_{n,0} + \sum_{i=1}^{m} c_{n,i}\Delta X_i + c_{n,m+1}\Delta S_{c_n} \qquad \overset{\triangleleft\triangleright}{c}_f = c_{f,0} + \sum_{i=1}^{m} c_{f,i}\Delta X_i + c_{f,m+1}\Delta S_{c_f} \qquad (21)$$

Therefore,

$$\overset{\triangleleft\triangleright}{c}^{0}_{eff} = \left(c_{n,0} + c_{f,0}\right)\cdot\left(1 + \sum_{i=1}^{m}\frac{\left(c_{n,i} + c_{f,i}\right)}{\left(c_{n,0} + c_{f,0}\right)}\cdot\Delta X_i + \frac{\sqrt{c_{n,m+1}^{\ 2} + c_{f,m+1}^{\ 2}}}{\left(c_{n,0} + c_{f,0}\right)}\cdot\Delta S^{0}_{c_{eff}}\right) \qquad (22)$$

We must calculate c_{eff} for the nominal condition of the circuit (i.e., any quantity in the circuit is at its nominal value) to get $c_{eff,0}$. Therefore, by using Eqns. (18), (20), and (22) the variational effective capacitance can be written as:

$$\overset{\triangleleft\triangleright}{c}_{eff} = c_{eff,0} + \sum_{i=1}^{m}\frac{\left(c_{n,i} + c_{f,i}\right)}{\left(c_{n,0} + c_{f,0}\right)}\cdot c_{eff,0}\,\Delta X_i + \frac{\sqrt{c_{n,m+1}^{\ 2} + c_{f,m+1}^{\ 2}}}{\left(c_{n,0} + c_{f,0}\right)}\cdot c_{eff,0}\,\Delta S_{c_{eff}} \qquad (23)$$

Now, we can use $\overset{\triangleleft\triangleright}{c}_{eff}$ in Eqn. (23) and the method presented in section 2.2 to generate the gate propagation delay and output slew time in the CFO form. However, this approach may not capture the effect of the variations of the resistance in the *RC*-π load on the gate timing analysis. Therefore, the next approach, finds *NSC*'s based on a reasonably accurate single-iteration c_{eff} calculation.

4.3.2 Finding $\overset{\triangleleft\triangleright}{c}_{eff}$ from $\overset{\triangleleft\triangleright}{c}^{1}_{eff}$

In this section we find the nominal value of the effective capacitance by performing iterative c_{eff} calculation for the nominal conditions of the circuit. Next we find *NSC*'s by applying a single-iteration effective capacitance method. c_{eff}^{1} means using single-iteration of Eqn. (5) as the gate load. Thus, $\overset{\triangleleft\triangleright}{c}^{1}_{eff}$ may be obtained by differentiating Eqn. (5) with respect to the sources of variations (c.f. section 2.2).

Subsequently, using the same approach as in section 4.1, we can find the $\overset{\triangleleft\triangleright}{c}_{eff}$ while the *NSC's* are calculated using the above single-iteration c_{eff} technique. Experimental results confirm that evaluating variational c_{eff} using the above approach shows an average error of 7% in the final delay and output slew time calculation with respect to Monte Carlo simulation.

5. Experimental Results

Our experiments use 90nm CMOS process parameters to model gates and interconnect parasitics. We assumed two different configurations for the experimental setup. The first one consists of two inverters connected in series whereas the second one is a CMOS inverter followed by a 2-input NAND gate. For both configurations, we apply a ramp input to the first inverter while its nominal value is chosen from the set $(t_{in})^{nom}$={10ps,80ps,150ps,220ps,300ps}. For the first configuration, size of the first inverter is fixed at W_p/W_n =30/15μm whereas size of the second inverter is chosen to be one of W_p/W_n={20/10, 50/25, 70/35, 100/50}μm. For the second configuration, size of the first inverter is again fixed at W_p/W_n =30/15μm whereas this time the size of the succeeding 2-input NAND gate is chosen to be one of W_p/W_n={40/40, 50/50, 100/100}μm.

To characterize the timing behavior of the gate, a look-up table based library is employed which represents the gate delay and output transition time as a function of input rise time, output capacitive load, V_{dd}, and temperature. We apply different loading scenarios for the second-stage gate as explained in the following subsections, i.e., pure capacitive load and general *RC* load. We have also

considered four different global sources of variation (V_{dd}, temperature, Metal layer 1 width, and ILD) and one independent random sources of variation for each electrical parameter (i.e., r and c) and timing parameter (for instance t_{in}) in the circuit. The sensitivity of each given data to the sources of variation is chosen randomly, while the total σ variation for each data is chosen to be 10% and 15% of their nominal value. We also assumed that the sources of variation are skewed with different skewness values as explained in each subsection. Mean, variance, and skewness of effective capacitance, the gate 50% propagation delay, and 10%-90% output transition time (slew time) are calculated using the approaches presented in this paper.

To compare the results, we ran Monte Carlo simulation with 10^4 samples on each test scenario and derived mean, variance, and skewness of effective capacitance, the gate 50% propagation delay, and 10%-90% output transition time. The average percentage errors for the mean, variance, and skewness of effective capacitance, the gate 50% propagation delay, and 10%-90% output transition time between the obtained results from the HSPICE and the calculated results based on using both VGTA and F-VGTA algorithm are reported.

A. Pure Capacitive Load

The load in this section is considered to be purely capacitive. Its nominal value is chosen to be $(C)^{nom}$= {400, 500, 800, 1400}fF. The scaled distribution of the sources of variation is considered to have a skewness of 0.4, 0.6, and 0.8. We performed our experiments on both circuit configurations explained above. The results for the first configuration (where the second gate is an inverter) are presented in Table 2 (the skewness of the given data is 0.4) and Table 3 (for the skewness of 0.8). The results for the second configuration are provided in Table 4 (for the skewness of 0.6). Experimental results indicate an average error of about 3% for two different σ values, i.e. 10% and 15%. As we increase the σ value (i.e. the total σ variation for each data; e.g. σ variation of t_{in}, and c_l) from 10% to 15%, the error in calculated mean, variance, and skewness of the delay and slew time increase, but slightly. The sources of error can be mainly classified into two groups: 1) the inaccuracy of the gate library table lookup and 2) the linear first order approximation of the timing

and electrical parameters with respect to the sources of variation. Note that, the runtime of the proposed algorithm in average is 129 times faster than the Monte Carlo based approach.

Table 2: Average error for the inverter driving pure capacitive load (Skewness=0.4)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew time**	**Delay**	**Slew time**
Mean	1.5%	1.7%	2.2%	2.3%
Variance	1.2%	1.3%	1.8%	1.9%
Skewness	1.0%	1.1%	1.4%	1.3%

Table 3: Average error for the inverter driving pure capacitive load (Skewness=0.8)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew time**	**Delay**	**Slew time**
Mean	1.9 %	2.3%	2.5%	2.9%
Variance	1.6%	1.7%	1.9%	2.1%
Skewness	1.4%	1.5%	1.5%	1.9%

Table 4: Average error for the 2-input NAND gate driving pure capacitive load (Skewness=0.6)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew time**	**Delay**	**Slew time**
Mean	3.0 %	3.1%	3.2%	3.1%
Variance	2.5%	2.7%	2.8%	2.9%
Skewness	2.2%	2.3%	2.5%	2.6%

B. General *RC* Load:

For this section, the load is considered to be an *RC* tree of varying topology. The nominal value of the total resistance of the load is chosen to be from the set $(R)^{nom}$= {150, 260, 300, 710, 1000}Ω and the nominal value of the total capacitance of the load is chosen to be from the set $(C)^{nom}$ ={400, 500, 800, 1400}*fF*. The scaled distribution of the sources of variation is considered to have a skewness of 0.5, 0.75, and 1.

Again, we performed the experiment on both circuit configurations as explained before. The results for the first configuration (where the second gate is an inverter) are presented in Table 5 (the skewness of the given data is 0.5) and Table 6 (the skewness of the given data is 0.75). The results for the second configuration are also provided in Table 7 (the skewness of the given data is 1). Experimental results indicate an average error of about 6% for different σ values. As we increase the σ value (i.e. the total σ variation for each data; e.g. σ variation of t_{in}, c_n, r_π, and c_f) from 10% to 15%, the error in calculated mean, variance, and skewness of c_{eff}, the gate delay, and output transition time increase, but slightly. Similarly, as skewness increases (e.g. skewness of t_{in}, c_n, r_π, and c_f) from 0.5 to 0.75, the error in calculated mean, variance, and skewness of the c_{eff}, as well as the error in delay and slew time increases, but slightly. The sources of error can be mainly classified into four groups: 1) the inaccuracy of the gate library table lookup, 2) the linear first order approximation of the timing and electrical parameters with respect to the sources of variation, 3) the error in calculating the variational *RC*-π load and 4) the error in the effective capacitance iterative equation proposed in section 4.1. Note that, the runtime of the proposed algorithm is, in average, 95 times faster than the Monte Carlo based approach.

Table 5: Average error for the inverter driving general *RC* load (Skewness=0.5)

	σ=10%	σ=15%

Average error	C_{eff}	Delay	Slew time	C_{eff}	Delay	Slew time
Mean	3.2%	3.5%	4.9%	3.5%	5.4%	5.8%
Variance	2.4%	3.3%	4.5%	2.6%	5.9%	5.2%
Skewness	2.5%	3.3%	4.9%	2.0%	5.5%	5.5%

Table 6: Average error for the inverter driving general *RC* load (Skewness=0.75)

	σ=10%			σ=15%		
Average error	C_{eff}	**Delay**	**Slew time**	C_{eff}	**Delay**	**Slew time**
Mean	3.5%	5.1 %	5.3%	3.8%	5.9%	6.1%
Variance	2.9%	4.3%	5.5%	3.6%	6.2%	6.2%
Skewness	2.8%	4.1%	4.9%	3.1%	5.9%	5.9%

Table 7: Average error for the 2-input NAND gate driving general *RC* load (Skewness=1)

	σ=10%			σ=15%		
Average error	C_{eff}	**Delay**	**Slew time**	C_{eff}	**Delay**	**Slew time**
Mean	4.1%	5.2 %	5.1%	4.2%	6.1%	6.7%
Variance	3.9%	5.4%	5.2%	4.3%	6.1%	6.1%
Skewness	4.0%	6.1%	5.6%	4.2%	6.5%	6.3%

For F-VGTA algorithm, again, we performed the experiment on both circuit configurations as explained before. The results for the first configuration (where the second gate is an inverter) are presented in Table 8 (when the C_{total} is used for calculating the *NSC*) and Table 9 (when the single iteration C_{eff} is used for calculating the NSC). The results for the second configuration are also

provided in Table 10 (when the C_{total} is used for calculating the *NSC*) and Table 11 (when the C_{total} is used for calculating the *NSC*). Experimental results indicate an average error of about 19% for different σ values when the c_{total} is used for calculating the *NSC*. It also shows an average error of about 7% for different σ values when the single iteration C_{eff} is used for calculating the *NSC*. As we increase the σ value (i.e. the total σ variation for each data; e.g. σ variation of t_{in}, c_n, r_π, and c_f) from 10% to 15%, the error in calculated mean and variance of C_{eff}, the gate delay, and output transition time increase, but slightly. The sources of error can be mainly classified into five groups: 1) the inaccuracy of the gate library table lookup, 2) the linear first order approximation of the timing and electrical parameters with respect to the sources of variation, 3) the error in calculating the variational *RC*-π load and 4) the error in the effective capacitance iterative equation. 5) the error in NSC approximation (Eqn. (20)). Note that, the runtime of the proposed algorithm is, in average, 185 times faster than the Monte Carlo based approach.

Table 8: Average error for the inverter driving general *RC* load when C_{total} is used for calculating *NSC*

	σ=10%		σ=15%	
Average error	**Delay**	**Slew time**	**Delay**	**Slew time**
Mean	14.6%	15.8%	18.1%	18.3%
Variance	15.4%	16.3%	16.9%	17.9%
Skewness	15.9%	17.5%	17.3%	18.5%

Table 9: Average error for the inverter driving general *RC* load when single iteration C_{eff} is used for calculating *NSC*

	σ=10%			σ=15%		
Average error	**Ceff**	**Delay**	**Slew time**	**Ceff**	**Delay**	**Slew time**
Mean	4.1%	6.5 %	6.7%	4.2%	6.4%	6.4%
Variance	3.9%	5.6%	6.0%	4.3%	6.5%	6.3%
Skewness	3.7%	5.1%	5.5%	4.4%	6.9%	6.4%

Table 10: Average error for the 2-input NAND gate driving general *RC* load when C_{total} is used for calculating *NSC*

	σ=10%		σ=15%	
Average error	**Delay**	**Slew time**	**Delay**	**Slew time**
Mean	16.6%	16.8%	19.1%	18.2%

Variance	16.4%	17.3%	17.9%	18.8%
Skewness	16.1%	17.7%	17.5%	19.0%

Table 11: Average error for the 2-input NAND gate driving general *RC* load when single iteration C_{eff} is used for calculating *NSC*

	σ=10%			σ=15%		
Average error	**Ceff**	**Delay**	**Slew time**	**Ceff**	**Delay**	**Slew time**
Mean	3.7%	5.6%	5.8%	4.6%	6.1%	6.2%
Variance	4.1%	5.4%	5.3%	4.5%	5.9%	5.8%
Skewness	4.5%	5.3%	5.2%	4.3%	5.6%	5.3%

6. Conclusion

In this paper we presented two frameworks to handle the variation-aware gate timing analysis in block-based σTA considering non-Gaussian sources of variation. To perform any of these frameworks, first, we proposed an approach to calculate variational *RC*-π load, which can be utilized instead of the actual variational *RC* load for the gate timing analysis purposes. Next, we presented a new approach for calculating effective capacitance in STA. We used this technique to calculate the statistical c_{eff} in canonical first-order (CFO) form, and thereby, calculated the gate delay and output slew time in the CFO form. Experimental results show an average error of 4% with respect to HSPICE Monte Carlo simulation.

7. References

[1] R. Nassif, "Modeling and Analysis of Manufacturing Variations," *CICC*, pp. 223-228, 2001.

[2] C. Visweswariah, K. Ravindran, K. Kalafala, S.G. Walker, S. Narayan, "First-order incremental block-based statistical timing analysis", Design Automation Conference, 2004. 41st , June 7-11, 2004, Pages:331 - 336

[3] H. Chang, V. Zolotov, S. Narayan, and C. Visweswariah "Parameterized Block-Based Statistical Timing Analysis with Non-Gaussian and Non-Linear Parameters," International Workshop on Timing Issues (TAU), 2005

[4] Y. Liu, L. T. Pileggi, and A. J. Strojwas, “Model Order Reduction of RC(L) Interconnect Including Variational Analysis,” DAC, pp. 201-206, 1999.

[5] J.D. MA and R.A. Rutenbar, “Interval-Valued Reduced Order Statistical Interconnect Modeling” , ICCAD, Pages:460-467, 2004.

[6] K. Agarwal, D. Sylvester, D. Blaauw, F. Liu, S. Nassif, S. Vrudhula, “Variational delay metrics for interconnect timing analysis,” Design Automation Conference, 41st , June 7-11, 2004 Pages:381 – 384, 2004.

[7] Agarwal, A.; Dartu, F.; Blaauw, D.;”Statistical gate delay model considering multiple input switching”, DAC Pages:658 – 663, 2004

[8] K. Okada, K. Yamaoka, H. Onodera, “A statistical gate-delay model considering intra-gate variability” Computer Aided Design, 2003. ICCAD-2003. International Conference on , 9-13 Nov. 2003 Pages:908 - 913

[9] V. Mehrotra, S. Nassif, D. Boning, and J. Chung, “Modeling the Effects of Manufacturing Variation on High-Speed Microprocessor Interconnect Performance,” *IEEE Electron Devices Meetings*, pp. 767-770, 1998.

[10] P.R. O’Brien and T. L. Savarino, “Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation,” Proc. of IEEE int’l Conf. on Computer Aided Design, pp.512-515, 1989

[11] A.B. Kahng, S. Muddu, ”Improved effective capacitance computations for use in logic and layout optimization,” VLSI Design, pp.578 – 582, 1999.

[12] F. Dartu, N. Menezes, and L. Pillegi, “Performance Computation for Precharacterized Gates with RC Loads”, IEEE Trans. On Computer Aided Design 15(5):544-533, 1996.

[13] S. Abbaspour, M. Pedram, “Calculating the Effective Capacitance for the RC Interconnect in VDSM Technologies,” ASPDAC, 2003.