Single-Source, Single-Destination Charge Migration in Hybrid Electrical Energy Storage Systems

Yanzhi Wang, *Student Member, IEEE*, Xue Lin, *Student Member, IEEE*, Younghyun Kim, *Member, IEEE*, Qing Xie, *Student Member, IEEE*, Massoud Pedram, *Fellow, IEEE*, and Naehyuck Chang, *Fellow, IEEE*

***Abstract*— In spite of extensive research it is still quite expensive to store electrical energy without converting it to a different form of energy. As of today, no single type of electrical energy storage (EES) element can fulfill all the desirable features of an ideal storage device, e.g., high-efficiency, high-power/energy capacity, low-cost, and long-cycle life. A hybrid EES system (HEES) consists of two or more heterogeneous EES elements, realizing the advantages of each EES element while hiding their weaknesses. HEES systems exhibit superior performance compared with homogeneous EES systems when appropriate charge allocation and replacement policies are developed and used. In addition, charge migration is mandatory because the optimal EES banks for charge allocation and replacement are in general different, and each EES bank has limited storage capacity. This paper formally describes the notion of charge migration efficiency and its optimization. We first define the charge migration architecture and the corresponding charge migration optimization problem. We provide a systematic solution for the single-source, single-destination charge migration problem considering the efficiency variation of the converters, the rate capacity and internal power loss of the storage element, the terminal voltage variation of the storage elements as a function of their state of charge, and so on. We also introduce the optimal solutions for both the time-constrained and -unconstrained versions of the charge migration problem formulations. Experimental results demonstrate significant charge migration efficiency improvement of up to 83.4%.**

***Index Terms*— Charge management, charge migration, hybrid electrical energy storage (HEES) system.**

I. Introduction

ELECTRICAL energy consumption largely fluctuates over time according to the variation of the load demands. Electricity supply and demand are commonly not balanced well with each other because typical fossil fuel and nuclear power plants can hardly respond to rapid changes in the load demand. Furthermore, the output power levels of most renewable power sources are largely dependent on the environmental factors such as solar irradiance and wind speed/direction. Power outage occurs if the electricity demand is larger than the supply. Power plant facilities should be large enough to provide the maximum electricity demand to prevent power outages. However, power planning to handle the maximum load demand results in energy inefficiency during the nonpeak hours. Instead, storage of excess energy during off-peak hours and compensation for the energy shortage during the peak hours is an alternative promising solution to mitigate the supply and demand mismatch. Electrical energy storage (EES) systems can thus increase power reliability and availability, compensate the supply demand mismatch, and regulate the peak-power demand. There are examples of practical deployment of a grid-scale EES system to mitigate the gap between the supply and demand [2], [3].

Electrical energy is a high-quality form of energy [4]–[6] that can be efficiently converted into other lower-quality forms of energy while generation of electrical energy from other forms of energy is less efficient in general. However, storing electrical energy is still expensive due to the limitation of the current EES (battery) technology. Most importantly, current EES systems are mainly homogeneous [3], i.e., they consist of a single type of EES elements, and therefore, suffer from the limitations inherited from that type of EES element.

Computer systems have the same limitation in bandwidth mismatch between high-capacity memory devices and microprocessors. Computer architectures adopt memory hierarchy consisting of L1 cache, L2 cache, L3 cache, DDR SDRAM main memory, flash nonvolatile storage, and hard disks instead of developing ultimate memory devices with both high-speed and -capacity, which is highly unlikely in a reasonable cost boundary. No single type of memory device can fulfill all the desirable requirements such as speed, capacity, cost, nonvolatility, power consumption, and so on., as of today or in the near future. The computer memory hierarchy consists of heterogeneous types of memory devices to hide drawbacks of each memory type while using their benefits. In parallel, a lot of research and development effort has focused on memory hierarchy management policies.

Like memory devices, no single EES element can fulfill all the requirements of EES and retrieval operations. It is not likely to have an ultimate high-efficiency, high-power/energy capacity, low-cost, and long-cycle life EES element any time

Manuscript received October 23, 2012; revised July 31, 2013; accepted November 21, 2013. This work was supported in part by the Software and Hardware Foundations of the Division of Computer and Communication Foundations of the U.S. National Science Foundation, in part by the Brain Korea 21 Project, in part by the National Research Foundation of Korea funded by the Korean Government under Grant 20120005640, and in part by The ICT at Seoul National University. *(Corresponding author: M. Pedram and N. Chang.)*

Y. Wang, X. Lin, Q. Xie, and M. Pedram are with the Department of Electrical Engineering, University of Southern California, Los Angeles, CA 90007 USA (e-mail: yanzhiwa@usc.edu; xuelin@usc.edu; xqing@usc.edu; pedram@usc.edu).

Y. Kim is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA (e-mail: yhkim1@purdue.edu).

N. Chang is with the Department of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-742, Korea (e-mail: naehyuck@elpl.snu.ac.kr).

Digital Object Identifier 10.1109/TVLSI.2013.2295050

soon. Therefore, a promising way to improve the performance of such EES systems is to exploit different types of EES elements with their unique strengths and weaknesses, and come up with the hybrid EES (HEES) system architecture and control policies that improve the key performance characteristics of the storage system. An HEES system is an EES system that consists of two or more heterogeneous EES elements. A simple structure of HEES systems is found in advanced electric vehicles, especially for efficient regenerative braking systems. More recently, generalized HEES systems are introduced [1], [7]–[13].

We require energy management policies for HEES systems, which are analogous to computer memory hierarchy management policies. The energy management policies can be separated into charge allocation, charge replacement, and charge migration operations [1], [7]. Charge allocation and replacement find the best-suited EES banks considering the input power or load demand and state of charge (SoC) of each EES bank [9], [11]. Unfortunately, the optimal charge allocation and charge replacement policies can hardly realize the best HEES system operation. The best-suited EES banks for charge allocation and charge replacement can be different with each other. Some types of EES banks are leaky and thus are not appropriate for long-term storage. Charge migration [1] moves charge from one EES element to another to improve the HEES system efficiency and responsiveness. Charge migration can ensure the availability of the best-suited EES bank(s) to receive power from an external power source, or to service a load demand. This means that the chosen EES bank(s) will have the desired characteristics (in terms of self-leakage, power rating) with respect to the power source or load demand.

This paper formally describes the notion of charge migration efficiency and its optimization. The contributions of this paper are summarized as follows: 1) a formal definition of the charge migration architecture and the corresponding charge migration problem formulation; 2) a systematic solution for the single-source, single-destination charge migration problem considering the efficiency variation of the converter, rate capacity effect and internal IR loss of the storage element, terminal voltage variation of the storage element as a function of the SoC, and so on; 3) formal statement of time-unconstrained and time-constrained charge migration optimization problems; 4) derivation of the optimal solution for the time-unconstrained problem, using offline-built lookup table to reduce the online computation effort; and 5) derivation of the optimal solution for the time-constrained problem based on dynamic programming.

II. HEES Systems

A. HEES System Architecture and Control

Fig. 1 shows the proposed HEES system architecture. The system consists of multiple heterogeneous EES banks. The EES banks are connected with each other through the charge transfer interconnect (CTI). Each EES bank consists of an EES (element) array and a bidirectional converter. The EES array is composed of multiple homogeneous EES elements with the same SoC and other characteristics, organized in a 2-D array

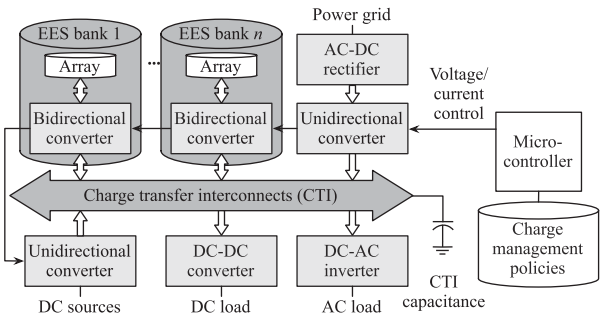


Fig. 1. Architecture of the proposed HEES system.

using series and/or parallel connections. Each EES array is incorporated with a current sensor for Coulomb counting, i.e., estimating the SoC of the EES array through integrating the charging/discharging current and accounting for the rate capacity effect. The bidirectional converters control power transfer into and out of the EES array through CTI regardless of their different voltages. The bidirectional converter is typically implemented based on a switching-mode power converter and can be configured as either a voltage regulator or a current regulator.

1) Voltage regulating mode: the converter generates a controllable voltage output. The target output voltage is set by a microcontroller of the HEES system. The converter compares the current output voltage with target voltage level, and adjusts its switching duty ratio through a feedback control loop to match the output voltage with the target voltage level. Current technologies enable a precise voltage regulation. For example, the LTM4607 converter has a maximum regulation inaccuracy of 0.5% [14], whereas the LTC4000 converter has a voltage regulation inaccuracy less than 0.25% [15].
2) Current regulating mode: the converter generates a controllable current output. Similarly, the target output current is set by the HEES microcontroller, and the converter adjusts its switching duty ratio through a feedback control loop to match output current with target current. The current regulation accuracy is also high. For example, the LTC4000 converter uses 12-bit resolution and has less than 1% regulation inaccuracy [15].

The HEES system has unidirectional converters for ac and dc power sources, or ac and dc loads.

We use a microcontroller as the main controller in the HEES system to determine the operation of the converters. At the beginning of each time slot of system operation, i.e., a decision epoch, it sets the target output voltage/current level of each converter according to the high-level charge management policies, and the target output voltage/current level of each converter will remain the same within the time slot (in the order of seconds). The power consumption of a typical ARM-based embedded processor or microcontroller is $0.6 \sim 1.2$ W [16], [17], which is much less than the incoming/output power of a typical HEES system, which is $50 \sim 100$ W.

This method enables us to control both the CTI voltage and the EES bank current. We set only one converter in the voltage regulating mode and let it control the CTI voltage

(using CTI capacitance). All others operate in the current regulating mode. The output current of the voltage regulating converter is automatically determined so that the sum of input currents of the CTI is equal to the sum of output currents. The other voltages and currents in the HEES system are associate variables and are determined due to energy conservation law once the output voltage/current level of each converter is set.

B. Charge Management for HEES Systems

As stated earlier, each EES element in existence today has its strengths and weaknesses in terms of the capital cost, cycle efficiency, cycle life, self-discharge rate, and power and energy densities. For example, a Li-ion battery bank provides high energy capacity, low self-discharge, stable open circuit terminal voltage, and relatively low cost, but suffers from a significant rate capacity effect. In contrast, a supercapacitor bank has superior cycle efficiency, a long cycle life, and capability of dealing with high power charging or discharging, but it has small energy capacity and high self-discharge rate. Therefore, it is crucial to determine which EES banks should be charged or discharged during the HEES system operation. The initial HEES work [7] introduced three mandatory charge management problems: charge allocation, charge replacement, and charge migration. The charge allocation problem finds appropriate destination EES banks and charging currents when energy comes from an external source, to maximize charging efficiency [9]. The charge replacement problem is to determine the appropriate source EES banks and discharging currents when there is a power demand from load device [11].

C. Charge Migration

Charge migration is the internal energy transfer among the EES banks. Even elaborated charge allocation and replacement policies cannot always guarantee that the best-suited EES banks are used for handling the incoming power supply or outgoing power demand because the best-suited EES banks for charge allocation can be different from the best-suited EES banks for charge replacement. Furthermore, the best-suited EES banks may not even be available for charge allocation or replacement due to the limited energy capacity of EES banks. In this context, appropriate charge migration can improve the energy efficiency of the HEES system by controlling the SoC of the EES banks for future charge allocation or replacement. For example, a future charge allocation may achieve the optimal efficiency when providing power for a particular EES bank. If such EES bank has full SoC at this moment, the future charge allocation cannot transfer the charge to that EES bank unless there is charge replacement from that bank in the mean time. Some EES elements are leaky and not appropriate for long-term storage. We should thus not let a leaky EES bank, e.g., a supercapacitor bank, store charge for a long period of time. We will be better off performing charge migration from the leaky EES bank to another EES bank for long-term storage if we foresee that the charge in the leaky bank will not be replaced in the near future.

In addition, charge migration can maximize the availability of the HEES system. Due to the lack of output power capacity, a HEES system may not be able to satisfy a load demand even if the total amount of energy in the HEES system is enough for the load demand. In other words, a HEES system may not be available for a high-power load demand if an EES bank with a high power capacity is empty, and another EES bank with a low power capacity has full SoC. If we are able to estimate the future load demand, we may perform charge migration in advance and make the HEES system available. In this paper, we primarily mention the charge migration problem to enhance the charge migration efficiency.

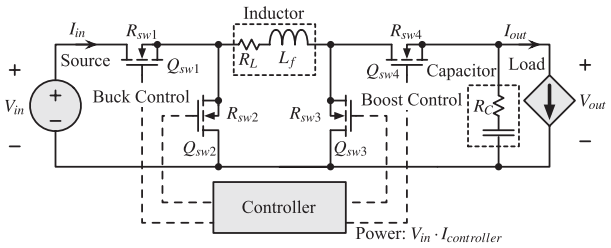


Fig. 2. Buck-boost switching converter circuit model.

III. HEES Component Models

A. Power Converters

We use a pulsewidth modulation (PWM) buck-boost switching converter as the converter in the HEES system to accommodate a wide range of EES array terminal voltages, with model shown in Fig. 2. We develop the converter power model based on the power model for buck switching converter provided in [18]. Efficiency of the converter is largely determined by its input voltage, input current, output voltage, and output current, denoted by V_{in}, I_{in}, V_{out}, and I_{out}, respectively. The converter efficiency η is defined as

$$\eta = \frac{V_{\text{out}} \cdot I_{\text{out}}}{V_{\text{in}} \cdot I_{\text{in}}} = \frac{V_{\text{in}} \cdot I_{\text{in}} - P_{\text{conv}}}{V_{\text{in}} \cdot I_{\text{in}}} \tag{1}$$

where P_{conv} is the power loss of the converter, which includes the conduction loss, the switching loss, the controller power loss, and the sensing power loss [14], [18]. Based on the relation between V_{in} and V_{out}, the converter has two working modes: the buck mode ($V_{\text{in}} > V_{\text{out}}$) and otherwise the boost mode. In the buck mode, the converter power loss P_{conv} is

$$\begin{aligned} P_{\text{conv}} = {} & {I_{\text{out}}}^2 \cdot (R_L + D \cdot R_{\text{sw1}} + (1-D) \cdot R_{\text{sw2}} + R_{\text{sw4}}) \\ & + \frac{(\Delta I)^2}{12} \cdot (R_L + D \cdot R_{\text{sw1}} + (1-D) \cdot R_{\text{sw2}} + R_{\text{sw4}} + R_C) \\ & + V_{\text{in}} \cdot f_s \cdot (Q_{\text{sw1}} + Q_{\text{sw2}}) + V_{\text{in}} \cdot I_{\text{controller}} + P_{\text{sense}} \end{aligned} \tag{2}$$

where $D = V_{\text{out}}/V_{\text{in}}$ is the PWM duty ratio and $\Delta I = V_{\text{out}} \cdot (1-D)/L_f \cdot f_s$ is the maximum current ripple, f_s is the switching frequency; $I_{\text{controller}}$ is the current flowing into the controller of the converter, R_L and R_C are the internal series resistances of the inductor L and the capacitor C, respectively, and R_{swi} and Q_{swi} are the turn-on resistance and gate charge of the ith MOSFET switch shown in Fig. 2, respectively. The first and second terms of (2) are dc and ac conduction losses, respectively; the third term is the switching loss; the fourth

term is the power loss of the converter's controller; and the last term P_{sense} is the sensing power loss.

If the converter is configured in the current regulating mode, the sensing power loss P_{sense} is given by

$$P_{\text{sense}} = (I_{\text{out}})^2 \cdot R_{\text{sense}} \tag{3}$$

where the current sensing resistance R_{sense} is a small resistance (not shown in Fig. 2), which is 18 mΩ for converter LTM4607 [14] or 10 mΩ for converter LTC4000 [15]. We can observe that the sensing power loss of a converter is smaller compared with the conduction power loss because $R_L = 39$ mΩ and $R_C = 300$ mΩ in a typical converter LTM4607 are much larger than R_{sense}. If the converter is configured in the voltage regulating mode, the sensing power loss is negligible [14]. The calculation of P_{sense} also applies to the boost mode.

In boost mode, the converter power loss P_{conv} is given by

$$\begin{aligned} P_{\text{conv}} = &\left(\frac{I_{\text{out}}}{1-D}\right)^2 \big(R_L + D \cdot R_{\text{sw3}} + (1-D)R_{\text{sw4}} + R_{\text{sw1}} \\ &+ D(1-D)R_C\big) \\ &+ \frac{(\Delta I)^2}{12} \cdot \big(R_L + D \cdot R_{\text{sw3}} + (1-D) \cdot R_{\text{sw4}} + R_{\text{sw1}} \\ &+ (1-D) \cdot R_C\big) \\ &+ V_{\text{out}} \cdot f_s \cdot (Q_{\text{sw3}} + Q_{\text{sw4}}) + V_{\text{in}} \cdot I_{\text{controller}} + P_{\text{sense}} \end{aligned} \tag{4}$$

where $D = 1 - V_{\text{in}}/V_{\text{out}}$ and $\Delta I = V_{\text{in}} \cdot D/L_f \cdot f_s$ in this case.

B. EES Element Array

We present a single-source, single-destination charge migration problem with two representative EES elements: Li-ion battery and supercapacitor, which can effectively explain fundamentals of charge migration without loss of generality. The two aforesaid EES elements have distinct characteristics from each other. Supercapacitors have the advantages of relatively high power capacity and low internal resistance, but disadvantages of low energy capacity, high self-discharge rate, and a wide range of voltage variation depending on SoC, compared with batteries. Table I summarizes the notations.

The voltaic representation of EES array SoC at time t is

$$V_{\text{SoC}}(t) = C_{\text{array}}(t)/C_{\text{full}} \times 1 \text{ V}. \tag{5}$$

We derive C_{full} in Coulomb from the nominal capacity Capacity given in Ahr

$$C_{\text{full}} = 3600 \times \text{Capacity}. \tag{6}$$

We interpret $V_{\text{SoC}}(t)$ as the state of an EES array.

EES array models specify the relationship among the SoC $V_{\text{SoC}}(t)$, the open circuit voltage (OCV) $V^{\text{OC}}_{\text{array}}(t)$, the closed circuit voltage (CCV) $V^{\text{CC}}_{\text{array}}(t)$, and the array current $I_{\text{array}}(t)$. Battery models for the electronic systems have been extensively studied during the past few decades [19]–[21]. As we are developing an mathematical formulation of the charge migration efficiency, a battery model in the form of an electric circuit is suitable for our purpose. We adopt the battery model introduced in [21], as shown in Fig. 3. This includes a runtime-based model on the left as well as a circuit-based model on the right for accurate capturing of the battery array service life and I–V characteristics. In Fig. 3, R_s, R_{ts} and R_{tl} are internal resistances, and C_{ts}, C_{tl} are internal capacitances, of the battery array. On the other hand, supercapacitors have a very low internal resistance (<1 mΩ). We introduce details of EES array models in the following three aspects: OCV-SoC relationship, CCV-OCV relationship, and rate capacity effect. Table II summarizes all the relationships.

TABLE I
NOTATIONS IN SECTION III-B

$V_{SOC}(t)$	SoC of an EES array
$C_{array}(t)$	Remaining charge in an EES array at time t
C_{full}	Total charge stored in EES array when fully charged
$Capacity$	Nominal capacity of an EES array
$V^{OC}_{array}(t)$	OCV of an EES array
$V^{CC}_{array}(t)$	CCV of an EES array
$I_{array}(t)$	Charging/discharging current of an EES array. $I_{array}(t) > 0$ implies that array is being charged
$V_{ts}(t)$, $V_{tl}(t)$	Voltage drops across internal capacitances
$\eta_{rate,c}(I_c)$	Charging efficiency of an EES array due to rate capacity effect when charging current is I_c
$\eta_{rate,d}(I_d)$	Discharging efficiency of EES array due to rate capacity effect when discharging current is I_d
k_c, α_c	Peukert constant of a battery array for charging
k_d, α_d	Peukert constant of battery array for discharging
$I_{eq}(t)$	Equivalent current inside an EES array, denoting charge accumulating/decreasing rate in that array

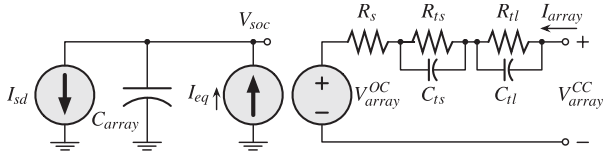


Fig. 3. Li-ion battery array equivalent circuit model.

1) OCV-SoC Relationship: $V^{\text{OC}}_{\text{array}}(t)$ is a monotonically increasing function of $V_{\text{SoC}}(t)$. $V^{\text{OC}}_{\text{array}}(t)$ is modeled as a voltage-controlled voltage source controlled by $V_{\text{SoC}}(t)$ of a battery array, as shown in Fig. 3. The OCV-SoC relationship is nonlinear and is given by

$$\begin{aligned} V^{\text{OC}}_{\text{array}}(t) = &\, b_1 e^{b_2 V_{\text{SoC}}(t)} + b_3 V_{\text{SoC}}(t)^3 + b_4 V_{\text{SoC}}(t)^2 \\ &+ b_5 V_{\text{SoC}}(t) + b_6 \end{aligned} \tag{7}$$

where those b_i's are empirically determined parameters from real pulsed charging and discharging measurements [22]. On the other hand, $V^{\text{OC}}_{\text{array}}(t)$ and $V_{\text{SoC}}(t)$ for a supercapacitor array satisfy a linear relationship.

2) CCV-OCV Relationship: $V^{\text{CC}}_{\text{array}}(t) \neq V^{\text{OC}}_{\text{array}}(t)$ when $I_{\text{array}}(t) \neq 0$ for the battery array due to internal resistances and capacitances. The relation between $V^{\text{CC}}_{\text{array}}(t)$ and $V^{\text{OC}}_{\text{array}}(t)$ of the battery array is

$$V^{\text{CC}}_{\text{array}}(t) = V^{\text{OC}}_{\text{array}}(t) + V_{\text{tl}}(t) + V_{\text{ts}}(t) + I_{\text{array}}(t) \cdot R_s. \tag{8}$$

TABLE II
SUMMARY OF EES ARRAY CHARACTERISTICS

Characteristics	Battery Array	Supercapacitor Array
OCV-SoC Relationship	Eqn. (7)	Linear Function
CCV-OCV Relationship	Eqn. (8)	$V^{CC}_{array}(t) \approx V^{OC}_{array}(t)$
Rate Capacity Effect	Eqn. (9)	$\eta_{rate,c}(I_c) \approx 1$, $\eta_{rate,d}(I_d) \approx 1$

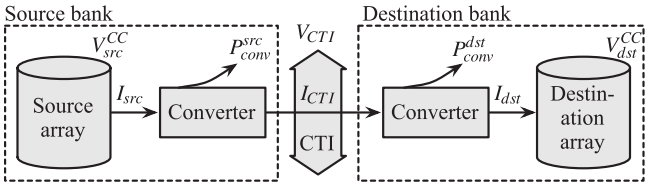


Fig. 4. Single-source, single-destination charge migration.

We have $V^{\rm CC}_{\rm array}(t) \approx V^{\rm OC}_{\rm array}(t)$ for a supercapacitor array due to its negligible internal resistance.

3) Rate Capacity Effect and Coulomb Counting: The rate capacity effect of batteries explains that the charging and discharging efficiencies decrease with the increasing of charging and discharging currents, respectively. More precisely, the Peukert's formula [23] describes that the charging and discharging efficiencies of a battery element array, as functions of the charging current I_c and discharging current I_d, respectively, are given by

$$\eta_{\rm rate,c}(I_c) = \frac{k_c}{(I_c)^{\alpha_c}}, \quad \eta_{\rm rate,d}(I_d) = \frac{k_d}{(I_d)^{\alpha_d}} \tag{9}$$

where k_c, α_c, k_d, and α_d are constants known *a priori*. We define the equivalent current inside the battery array as the actual charge accumulating/reducing speed

$$I_{\rm eq}(t) = \begin{cases} I_{\rm array}(t) \cdot \eta_{\rm rate,c}(I_{\rm array}(t)), & \text{if } I_{\rm array}(t) > 0 \\ I_{\rm array}(t)/\eta_{\rm rate,d}(|I_{\rm array}(t)|), & \text{if } I_{\rm array}(t) < 0. \end{cases} \tag{10}$$

In contrast, the rate capacity effect of supercapacitor is negligible, i.e., $I_{\rm eq}(t) \approx I_{\rm array}(t)$.

We calculate $V_{\rm SoC}(t)$ from the initial SoC $V_{\rm SoC}(T_0)$ ($T_0 < t$) using Coulomb counting

$$V_{\rm SoC}(t) = V_{\rm SoC}(T_0) + \frac{\int_{T_0}^{t} I_{\rm eq}(\tau) d\tau}{C_{\rm full}}. \tag{11}$$

IV. PROBLEM FORMULATION

We focus on the optimal single-source, single-destination charge migration. Fig. 4 shows the conceptual architecture of a single-source, single-destination charge migration process. During charge migration, the converter in the source EES bank is configured as the voltage regulating mode and properly maintains the CTI voltage. The converter in the destination EES bank is configured as the current regulating mode. The central HEES microcontroller sets the target output voltage or current of programmable converters at each decision epoch. Table III summarizes the notations.

TABLE III
NOTATIONS FOR CHARGE MIGRATION FORMULATION

$V^{src}_{SOC}(t)$, $V^{dst}_{SOC}(t)$	SoC of source and destination EES arrays
$V^{OC}_{src}(t)$, $V^{OC}_{dst}(t)$	OCV of source and destination EES arrays
$V^{CC}_{src}(t)$, $V^{CC}_{dst}(t)$	CCV of source and destination EES arrays
$V_{CTI}(t)$	CTI voltage
$I_{src}(t)$	Discharging current of the source EES array
$I_{dst}(t)$	Charging current of the destination EES array
$I_{CTI}(t)$	Migration current on the CTI
$P^{src}_{conv}(t)$	Power loss of converter in the source EES bank
$P^{dst}_{conv}(t)$	Power loss of converter in destination bank
T_0	Start time of the charge migration process
T_d	Relative deadline of the charge migration process
$\eta^{src}_{rate,d}(I_{src}(t))$	Discharging efficiency of source EES array due to rate capacity effect when discharging current is $I_{src}(t)$
$\eta^{dst}_{rate,c}(I_{dst}(t))$	Charging efficiency of destination EES array due to rate capacity effect when charging current is $I_{dst}(t)$
C^{src}_{full}	Total charge stored in the source EES array when it is fully charged
C^{dst}_{full}	Total charge stored in the destination EES array when it is fully charged
Q	Amount of charge to be migrated
$S \xrightarrow{Q} D$	Single-source, single-destination charge migration problem
$S \xrightarrow[[T_0,\infty]]{Q} D$	Time-unconstrained $S \xrightarrow{Q} D$
$S \xrightarrow[[T_0,T_0+T_d]]{Q} D$	Time-constrained $S \xrightarrow{Q} D$
η_{GME}	Global migration efficiency
η_{IME}	Instantaneous migration efficiency
$I_{dst,opt}(t)$	Optimal $I_{dst}(t)$ that maximizes η_{IME} at time t
$V_{CTI,opt}(t)$	Optimal $V_{CTI}(t)$ that maximizes η_{IME}
Δ_T	Duration of a time slot
Δq_i	The optimal amount of charge migrated to the destination array in time slot i
Min_Loss	Matrix for dynamic programming in Algorithm 1
Last_Chg	Matrix for tracing back in Algorithm 1
$C_{drawn}(q', q, i)$	The minimum amount of charge drawn from the source EES array during time slot i to deliver $q - q'$ to the destination EES array
$V_{CTI,opt}(I_{dst}(t))$	Optimal $V_{CTI}(t)$ that maximizes η_{IME} for given $I_{dst}(t)$ at time t
$\hat{V}_{CTI,opt}(I_{dst}(t))$	Fitted value of $V_{CTI,opt}(I_{dst}(t))$

The single-source, single-destination charge migration problem is constrained by the energy conservation law. As shown in Fig. 4, the power flowing into the destination EES bank charges the corresponding EES element array and drives the corresponding converter

$$V_{\rm CTI}(t) \cdot I_{\rm CTI}(t) = P^{\rm dst}_{\rm conv}(t) + V^{\rm CC}_{\rm dst}(t) \cdot I_{\rm dst}(t) \tag{12}$$

where $V_{\rm CTI}(t)$ and $I_{\rm CTI}(t)$ are the CTI voltage and the migration current on the CTI, respectively. The destination array CCV $V^{\rm CC}_{\rm dst}(t)$ is a strong function of its OCV $V^{\rm OC}_{\rm dst}(t)$ and charging current $I_{\rm dst}(t)$. The CCV-OCV relationship of EES arrays captures their relationship. The migration current on the CTI comes from the source EES array through the

corresponding converter

$$V_{\mathrm{CTI}}(t) \cdot I_{\mathrm{CTI}}(t) = V_{\mathrm{src}}^{\mathrm{CC}}(t) \cdot I_{\mathrm{src}}(t) - P_{\mathrm{conv}}^{\mathrm{src}}(t) \quad (13)$$

where the source array CCV $V_{\mathrm{src}}^{\mathrm{CC}}(t)$ is a strong function of its OCV $V_{\mathrm{src}}^{\mathrm{OC}}(t)$ and discharging current $I_{\mathrm{src}}(t)$. The converter power loss values $P_{\mathrm{conv}}^{\mathrm{dst}}(t)$ and $P_{\mathrm{conv}}^{\mathrm{src}}(t)$ are functions of the input voltage, output voltage, and output current of the corresponding converters, as described in Section III-A.

Suppose that the charge migration process starts at time $T_0 = 0$ and ends at time $T_0 + T_d$. The HEES controller provides set points of the two variables $V_{\mathrm{CTI}}(t)$ and $I_{\mathrm{dst}}(t)$ for $t \in [T_0, T_0 + T_d]$. The HEES system calculates the SoC values $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ using Coulomb counting

$$V_{\mathrm{SoC}}^{\mathrm{src}}(t) = V_{\mathrm{SoC}}^{\mathrm{src}}(T_0) - \frac{\int_{T_0}^{t} I_{\mathrm{src}}(\tau)/\eta_{\mathrm{rate},d}^{\mathrm{src}}(I_{\mathrm{src}}(\tau))d\tau}{C_{\mathrm{full}}^{\mathrm{src}}} \quad (14)$$

$$V_{\mathrm{SoC}}^{\mathrm{dst}}(t) = V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0) + \frac{\int_{T_0}^{t} I_{\mathrm{dst}}(\tau) \cdot \eta_{\mathrm{rate},c}^{\mathrm{dst}}(I_{\mathrm{dst}}(\tau))d\tau}{C_{\mathrm{full}}^{\mathrm{dst}}}. \quad (15)$$

$V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ depend on control variable values $V_{\mathrm{CTI}}(\tau)$ and $I_{\mathrm{dst}}(\tau)$ for $\tau \in [T_0, t)$. We calculate $V_{\mathrm{src}}^{\mathrm{OC}}(t)$ and $V_{\mathrm{dst}}^{\mathrm{OC}}(t)$ based on the OCV-SoC relationship of source and destination EES arrays, respectively. The rest of variables shown in Fig. 4 are either given or associated variables, which are determined by control variables and (12) and (13).

We formally describe the time-unconstrained charge migration problem $S \xrightarrow[[T_0,\infty]]{Q} D$ and time-constrained charge migration problem $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ as an optimal control problem considering efficiency variations of both converters, rate capacity effect, and OCV variations of the EES element arrays. The power dissipation of the HEES microcontroller and peripherals is not accounted for in the problem formulation since they are not dedicated for the charge migration process. We will discuss their power dissipation in Section VII.

1) Given: the initial SoC $V_{\mathrm{SoC}}^{\mathrm{src}}(T_0)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0)$, the amount of charge to be migrated Q[1] and the relative deadline T_d, where $T_d = \infty$ in $S \xrightarrow[[T_0,\infty]]{Q} D$.
2) Find: the optimal $V_{\mathrm{CTI}}(t)$ and $I_{\mathrm{dst}}(t)$ for $t \in [T_0, T_0+T_d]$ during the charge migration process.
3) Such that: $\int_{T_0}^{T_0+T_d} I_{\mathrm{dst}}(t) \cdot \eta_{\mathrm{rate,c}}^{\mathrm{dst}}(I_{\mathrm{dst}}(t))dt = Q$. In addition, the global migration efficiency (GME) should be maximized, which is given by

$$\eta_{\mathrm{GME}} = \frac{\int_{T_0}^{T_0+T_d} V_{\mathrm{dst}}^{\mathrm{OC}}(t) \cdot I_{\mathrm{dst}}(t) \cdot \eta_{\mathrm{rate,c}}^{\mathrm{dst}}(I_{\mathrm{dst}}(t))dt}{\int_{T_0}^{T_0+T_d} V_{\mathrm{src}}^{\mathrm{OC}}(t) \cdot I_{\mathrm{src}}(t)/\eta_{\mathrm{rate,d}}^{\mathrm{src}}(I_{\mathrm{src}}(t))dt}. \quad (16)$$

Please note that the CTI voltage V_{CTI} may at some time be a constant value predefined by the system, due to potential compliance to standards, compatibility choices, and stability issues. In this case, only $I_{\mathrm{dst}}(t)$ for $t \in [T_0, T_0 + T_d]$ will be the optimization variable in the charge migration process, and we still maximize the GME given by (16) satisfying

$$\int_{T_0}^{T_0+T_d} I_{\mathrm{dst}}(t) \cdot \eta_{\mathrm{rate,c}}^{\mathrm{dst}}(I_{\mathrm{dst}}(t))dt = Q.$$

V. Time-Unconstrained Charge Migration

A. Instantaneous Migration Efficiency Optimization

We consider the instantaneous migration efficiency (IME) in $S \xrightarrow[[T_0,\infty]]{Q} D$ at time t. We consider the general problem where both $V_{\mathrm{CTI}}(t)$ and $I_{\mathrm{dst}}(t)$ are optimization variables. We obtain $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ from Coulomb counting. We have two control variables $I_{\mathrm{dst}}(t)$ and $V_{\mathrm{CTI}}(t)$. This problem is a specific case of the general problem stated in Section IV as $T_d \to 0$. We maximize the IME such that

$$\max_{I_{\mathrm{dst}}(t), V_{\mathrm{CTI}}(t)} \eta_{\mathrm{IME}}\left(I_{\mathrm{dst}}(t), V_{\mathrm{CTI}}(t)\right) = \max_{I_{\mathrm{dst}}(t), V_{\mathrm{CTI}}(t)} \frac{V_{\mathrm{dst}}^{\mathrm{OC}}(t) \cdot I_{\mathrm{dst}}(t) \cdot \eta_{\mathrm{rate,c}}^{\mathrm{dst}}(I_{\mathrm{dst}}(t))}{V_{\mathrm{src}}^{\mathrm{OC}}(t) \cdot I_{\mathrm{src}}(t)/\eta_{\mathrm{rate,d}}^{\mathrm{src}}(I_{\mathrm{src}}(t))}. \quad (17)$$

The optimal control variable values $I_{\mathrm{dst,opt}}(t)$ and $V_{\mathrm{CTI,opt}}(t)$ are given by

$$\left(I_{\mathrm{dst,opt}}(t), V_{\mathrm{CTI,opt}}(t)\right) = \underset{(I_{\mathrm{dst}}(t), V_{\mathrm{CTI}}(t))}{\arg\max} \eta_{\mathrm{IME}}\left(I_{\mathrm{dst}}(t), V_{\mathrm{CTI}}(t)\right). \quad (18)$$

$I_{\mathrm{dst,opt}}(t)$ and $V_{\mathrm{CTI,opt}}(t)$ are functions of $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$. Maximization of the IME is in general a quasi-convex (unimodal) optimization problem over $I_{\mathrm{dst}}(t)$ and $V_{\mathrm{CTI}}(t)$. The IME becomes lower when $I_{\mathrm{dst}}(t) > I_{\mathrm{dst,opt}}(t)$ due to increasing in power dissipation caused by the EES array internal resistance and rate capacity effect. The IME becomes lower when $I_{\mathrm{dst}}(t) < I_{\mathrm{dst,opt}}(t)$ because of the converter efficiency degradation. We exploit a ternary search algorithm, which is an extension of the well-known binary search algorithm, utilizing this quasi-convex property. This makes the solution quickly converge to the global optimal or at least a near global optimal solution. A branch and bound method provides the global optimal solution of the IME optimization problem at the expense of the solution complexity. We have the following observation about $I_{\mathrm{dst,opt}}(t)$.

Observation 1: $I_{\mathrm{dst,opt}}(t)$ becomes relatively larger when $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ is higher and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ is lower. ■

B. GME Optimization

We derive the optimal solution of $S \xrightarrow[[T_0,\infty]]{Q} D$ that maximizes η_{GME} in (16). Charge migration makes $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$ decrease and $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ increase as time elapses. We solve $S \xrightarrow[[T_0,\infty]]{Q} D$ in a discrete time space. We divide the charge migration process into time slots with an equal distance Δ_T. We calculate $V_{\mathrm{SoC}}^{\mathrm{src}}(T_0 + i\,\Delta_T)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0 + i\,\Delta_T)$ at each decision epoch $T_0 + i\,\Delta_T$, which is the beginning of each time slot, using the Coulomb counting method given in (14) and (15). We maximize the IME and find $I_{\mathrm{dst,opt}}(T_0 +$

[1]Due to power loss during charge migration, the amount of charge extracted from the source EES array is greater than that transferred to the destination EES array. We use the reference amount of charge that is eventually transferred to the destination EES array in this paper

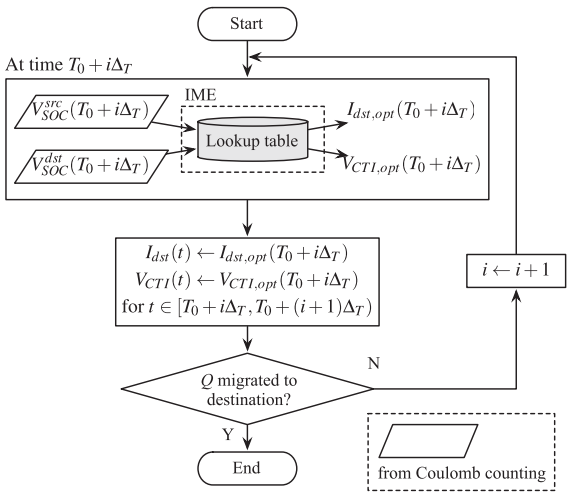


Fig. 5. Online procedure in the optimal solution of $S \xrightarrow[[T_0,\infty]]{Q} D$ that maximizes η_{GME}. The lookup table is built offline.

$i\,\Delta_T$) and $V_{\text{CTI,opt}}(T_0 + i\,\Delta_T)$. We set $I_{\text{dst}}(t) = I_{\text{dst,opt}}(T_0 + i\,\Delta_T)$ and $V_{\text{CTI}}(t) = V_{\text{CTI,opt}}(T_0 + i\,\Delta_T)$ during the time slot. We continue this process until Q is migrated into the destination EES array. We avoid from $I_{\text{dst}}(t)$ and $V_{\text{CTI}}(t)$ changing abruptly within two consecutive time slots by setting Δ_T small enough. In this case, the proposed solution is the optimal solution.

We reduce the online computation overhead by separating the solution into offline and online phases. We build a lookup table offline. The input variables of the lookup table are $V^{\text{src}}_{\text{SoC}}(t)$ and $V^{\text{dst}}_{\text{SoC}}(t)$, and the values stored in the lookup table are $V_{\text{CTI,opt}}(t)$ and $I_{\text{dst,opt}}(t)$. The online phase only needs to index the lookup table with $V^{\text{src}}_{\text{SoC}}(T_0 + i\,\Delta_T)$ and $V^{\text{dst}}_{\text{SoC}}(T_0 + i\,\Delta_T)$ at each decision epoch $T_0 + i\,\Delta_T$ to find the optimal control variable values. Since there are only two input variables, the size of the lookup table does not grow much. Experimental results also back up that the granularity level of the lookup table does not have a strong effect on the charge migration efficiency. The online procedure is shown in Fig. 5.

Fig. 6 shows an example of the optimal solution of $S \xrightarrow[[T_0,\infty]]{Q} D$. The source and destination EES banks are both supercapacitor banks with the initial OCVs of $V^{\text{OC}}_{\text{src}}(T_0) = 8$ V and $V^{\text{OC}}_{\text{dst}}(T_0) = 4$ V, respectively. The traces of $V^{\text{OC}}_{\text{src}}(t)$, $V^{\text{OC}}_{\text{dst}}(t)$ and $I_{\text{dst}}(t) = I_{\text{dst,opt}}(t)$ are shown in Fig. 6.

VI. Time-Constrained Charge Migration

A. Optimal Solution

We derive the optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ based on dynamic programming. We consider the general problem where both $V_{\text{CTI}}(t)$ and $I_{\text{dst}}(t)$ are optimization variables. We begin with the following theorem. Please refer to the Appendix for detailed proof.

Theorem 1: Maximizing η_{GME} in (16) is equivalent to minimizing the total amount of charge extracted from the source EES array, which is given by $\int_{T_0}^{T_0+T_d} I_{\text{src}}(t)/\eta^{\text{src}}_{\text{rate,d}}(I_{\text{src}}(t))dt$.

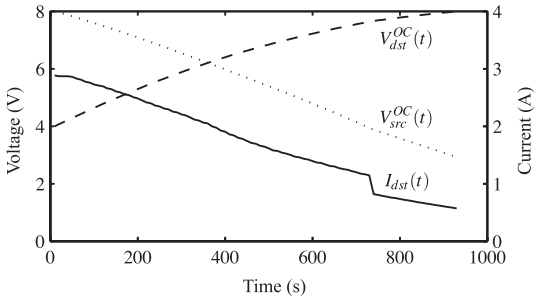


Fig. 6. Example of optimal time-unconstrained charge migration.

We find the optimal substructure property of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ as follows. This enables us to apply dynamic programming to find the optimal solution of the problem.

Property 1 *(The Optimal Substructure Property):* Suppose, we achieve the optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ that maximizes η_{GME}. Suppose that Q' ($Q' \leq Q$) is migrated to the destination EES array by $T_0 + T'_d$ ($T'_d < T_d$) in the optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$. This corresponds to the subproblem $S \xrightarrow[[T_0,T_0+T'_d]]{Q'} D$. The optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ contains within it the optimal solution of the subproblem $S \xrightarrow[[T_0,T_0+T'_d]]{Q'} D$. ■

Based on Property 1, we introduce the optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$. The optimal solution is comprised of a planning phase and a control phase. The planning phase is executed at time T_0, i.e., the beginning of charge migration, to find the optimal amount of charge migrated to the destination array in each time slot, denoted by Δq_1, Δq_2, …, Δq_N. On the other hand, the control phase is executed along with the charge migration process to determine the optimal $V_{\text{CTI}}(t)$ and $I_{\text{dst}}(t)$ for $t \in [T_0, T_0 + T_d]$ and control the process. We will discuss the two phases in details as follows.

1) Planning Phase: The optimal algorithm in the planning phase is based on dynamic programming and given in Algorithm 1, which requires to take a holistic view of the whole charge migration process at the beginning of the process.

For $0 \leq q \leq Q$ and $0 \leq i \leq N$, let Min_Loss(q, i) denote the minimal amount of charge drawn from the source EES array during $[T_0, T_0 + i\,\Delta_T]$ when we migrate q to the destination EES array during that time period. We initialize Min_Loss(q, i) as

$$\text{Min\_Loss}(q,i) = \begin{cases} 0, & \text{for } q = 0 \\ \infty, & \text{for } q > 0 \end{cases} \tag{19}$$

for $0 \leq i \leq N$. We calculate Min_Loss$(q, i+1)$ from all the Min_Loss(q', i) for $0 \leq q' \leq q$ based on Property 1. We calculate Min_Loss$(q, i+1)$ in two steps as follows. We keep the control variables, i.e., $I_{\text{dst}}(t)$ and $V_{\text{CTI}}(t)$, the same within the time slot $i + 1$.

Algorithm 1 Planning Phase for the Time-Constrained Charge Migration Problem Using Dynamic Programming

Input: Initial SoC $V_{SOC}^{src}(T_0)$ and $V_{SOC}^{dst}(T_0)$, Q, and T_d
Output: Δq_1, Δq_2, ..., Δq_N
Initialize Min_Loss$(q=0, i=0) \leftarrow 0$ and
Min_Loss$(q, i=0) \leftarrow \infty$ for $\forall q > 0$
for $(i=0; i<N; i++)$ **do**
  for $(q=0; q \le Q; q = q + \frac{Q}{M})$ **do**
    for $(q'=0; q' \le q; q' = q' + \frac{Q}{M})$ **do**
      Calculate $C_{drawn}(q', q, i+1)$ in the way as shown in Step I
    Calculate **Min_Loss**$(q, i+1)$ and **Last_Chg**$(q, i+1)$ as shown in Step II
Perform tracing back using the **Min_Loss** and **Last_Chg** matrices to determine the Δq_1, Δq_2, ..., Δq_N values

Step 1 (Calculation of $C_{\text{drawn}}(q', q, i+1)$ *for* $0 \le q' \le q$*):* The following equation calculates $I_{\text{dst}}(t)$ for $t \in [T_0 + i\Delta_T, T_0 + (i+1)\Delta_T)$ that guarantees the destination EES array to accumulate $q - q'$ in the time slot $i+1$:

$$I_{\text{dst}}(t) \cdot \eta^{\text{dst}}_{\text{rate,c}}(I_{\text{dst}}(t)) = \frac{q - q'}{\Delta_T}. \tag{20}$$

We calculate $V^{\text{src}}_{\text{SoC}}(T_0 + i\Delta_T)$ based on $V^{\text{src}}_{\text{SoC}}(T_0)$ and Min_Loss(q', i), and calculate $V^{\text{dst}}_{\text{SoC}}(T_0 + i\Delta_T)$ based on $V^{\text{dst}}_{\text{SoC}}(T_0)$ and q'

$$V^{\text{src}}_{\text{SoC}}(T_0 + i\Delta_T) = V^{\text{src}}_{\text{SoC}}(T_0) - \frac{\text{Min\_Loss}(q', i)}{C^{\text{src}}_{\text{full}}} \tag{21}$$

$$V^{\text{dst}}_{\text{SoC}}(T_0 + i\Delta_T) = V^{\text{dst}}_{\text{SoC}}(T_0) + \frac{q'}{C^{\text{dst}}_{\text{full}}}. \tag{22}$$

We find $V_{\text{CTI,opt}}(I_{\text{dst}}(T_0 + i\Delta_T))$ that maximizes the IME at $T_0 + i\Delta_T$ with given $V^{\text{src}}_{\text{SoC}}(T_0 + i\Delta_T)$, $V^{\text{dst}}_{\text{SoC}}(T_0 + i\Delta_T)$, and $I_{\text{dst}}(T_0 + i\Delta_T)$, using optimization methods such as ternary search or branch and bound, or the high-order curve fitting method, as shall be discussed in Section VI-B. We set $V_{\text{CTI}}(t) = V_{\text{CTI,opt}}(I_{\text{dst}}(T_0 + i\Delta_T))$ for $t \in [T_0 + i\Delta_T, T_0 + (i+1)\Delta_T)$. We calculate $C_{\text{drawn}}(q', q, i+1)$, which is the minimum amount of charge drawn from source EES array during time slot $i+1$ to deliver $q - q'$ to destination array, using (8) and (12)–(14). ∎

Step 2 (Calculation of Min_Loss$(q, i+1)$*):* We calculate Min_Loss$(q, i+1)$ as follows:

$$\text{Min\_Loss}(q, i+1) = \min_{0 \le q' \le q} \{\text{Min\_Loss}(q', i) + C_{\text{drawn}}(q', q, i+1)\}. \tag{23}$$

We keep track of the optimal q'

$$\text{Last\_Chg}(q, i+1) = \arg\min_{0 \le q' \le q} \{\text{Min\_Loss}(q', i) + C_{\text{drawn}}(q', q, i+1)\} \tag{24}$$

which is necessary in finding the optimal control variable values after we find Min_Loss(Q, N). ∎

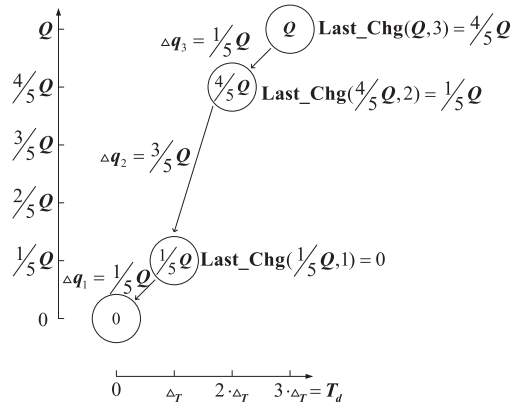


Fig. 7. Example to illustrate the tracing back procedure.

After we find Min_Loss(Q, N) and Last_Chg(Q, N), we determine the optimal amount of charge migrated to the destination array in each time slot, denoted by Δq_1, Δq_2, …, Δq_N, in a reverse chronological order. For example, the optimal amount of migrated charge in time slot N is $\Delta q_N = Q - \text{Last\_Chg}(Q, N)$, and that in time slot $N-1$ is $\Delta q_{N-1} = Q - \Delta q_N - \text{Last\_Chg}(Q - \Delta q_N, N-1)$. This process is called tracing back in dynamic programming [24]. We use Fig. 7 as an example to illustrate the tracing back procedure with $N = 3$. In this example we have migrated Q amount of charge by the end of the third time slot. We have Last_Chg$(Q, N=3) = 4/5Q$, which is the optimal amount of charge migrated by the end of the second time slot. Then, we have $\Delta q_3 = Q - \text{Last\_Chg}(Q, 3) = 1/5Q$. Furthermore, we have Last_Chg$(4/5Q, 2) = 1/5Q$, which is the optimal amount of charge migrated by the end of the first time slot, and then $\Delta q_2 = 4/5Q - \text{Last\_Chg}(4/5Q, 2) = 3/5Q$. Finally, because no charge has been migrated to the destination array at the beginning of the first time slot, we have $\Delta q_1 = 1/5Q - 0 = 1/5Q$.

2) Control Phase: Now that we have determined the set of Δq_1, Δq_2,…, Δq_N values from the tracing back procedure. At each decision epoch $T_0 + i\Delta_T$ in the actual charge migration process, we calculate $V^{\text{src}}_{\text{SoC}}(T_0 + i\Delta_T)$ and $V^{\text{dst}}_{\text{SoC}}(T_0 + i\Delta_T)$ using the Coulomb counting method given in (14) and (15). We determine the $I_{\text{dst}}(t)$ value during the time slot $[T_0 + i\Delta_T, T_0 + (i+1)\Delta_T)$, such that Δq_{i+1} amount of charge can be migrated into the destination EES array

$$I_{\text{dst}}(t) \cdot \eta^{\text{dst}}_{\text{rate,c}}(I_{\text{dst}}(t)) = \Delta q_{i+1}/\Delta_T. \tag{25}$$

We subsequently determine the optimal $V_{\text{CTI,opt}}(I_{\text{dst}}(T_0 + i\Delta_T))$ that maximizes the IME at $T_0 + i\Delta_T$ with given $V^{\text{src}}_{\text{SoC}}(T_0 + i\Delta_T)$, $V^{\text{dst}}_{\text{SoC}}(T_0 + i\Delta_T)$, and the just calculated $I_{\text{dst}}(T_0 + i\Delta_T)$. We find the optimal CTI voltage value through branch and bound or ternary search algorithm, or the high-order curve fitting method that will be discussed in Section VI-B. We set $I_{\text{dst}}(t) = I_{\text{dst}}(T_0 + i\Delta_T)$ and $V_{\text{CTI}}(t) = V_{\text{CTI,opt}}(I_{\text{dst}}(T_0 + i\Delta_T))$ during the time slot $[T_0 + i\Delta_T, T_0 + (i+1)\Delta_T)$ to control charge migration, and wait until the next time slot $T_0 + (i+1)\Delta_T$.

B. High-Order Curve Fitting

The optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ requires finding $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ with given $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$, $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$, and $I_{\mathrm{dst}}(t)$ in both the planning phase and the control phase. To reduce the online computation overhead, we use a high-order curve fitting method to find an approximation of $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$. We use a kernel feature vector $\mathcal{K}(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t))$ in the high-order curve fitting, which is a collection of high-order functions of $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$, $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$, and $I_{\mathrm{dst}}(t)$. The kernel feature vectors have been widely used in machine learning methods [25]. We approximate $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ by a linear function of $\mathcal{K}(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t))$

$$\hat{V}_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t)) = \theta(0) + [\theta(1), \theta(2), \ldots, \theta(n)] \cdot \mathcal{K}(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t)) \tag{26}$$

where $\Theta = [\theta(0), \theta(1), \ldots, \theta(n)]$ is the fitting parameter vector with $n+1$ elements to be determined by the offline training phase of the high-order curve fitting. The high-order curve fitting method acts better than traditional linear curve fitting in capturing the nonlinear relationship between $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ and $(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t))$ as pointed out in [25]. The following kernel feature vector yields the best fitting results:

$$\begin{aligned}&\mathcal{K}(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t))\\ &=\big[V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t), (V_{\mathrm{SoC}}^{\mathrm{src}}(t))^2, (V_{\mathrm{SoC}}^{\mathrm{dst}}(t))^2, (I_{\mathrm{dst}}(t))^2,\\ &\quad V_{\mathrm{SoC}}^{\mathrm{src}}(t)\cdot V_{\mathrm{SoC}}^{\mathrm{dst}}(t), V_{\mathrm{SoC}}^{\mathrm{src}}(t)\cdot I_{\mathrm{dst}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t)\cdot I_{\mathrm{dst}}(t)\big]^T.\end{aligned} \tag{27}$$

We set $n = 9$ as the kernel feature vector has nine elements. Hence, there are ten fitting parameters in total including the constant term of $\theta(0)$.

The proposed high-order curve fitting method consists of both an offline initial training phase and an online estimation phase. The initial training phase determines $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ with an optimization method such as branch and bound or ternary search algorithm for each possible $(V_{\mathrm{SoC}}^{\mathrm{src}}(t), V_{\mathrm{SoC}}^{\mathrm{dst}}(t), I_{\mathrm{dst}}(t))$ pair. We determine Θ using a standard least square method [25]. The online estimation phase calculates $\hat{V}_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ for given $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$, $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ and $I_{\mathrm{dst}}(t)$ from (26). We use separate high-order curve fitting with different set of fitting parameters for the buck mode ($V_{\mathrm{src}}^{\mathrm{OC}}(t) > V_{\mathrm{dst}}^{\mathrm{OC}}(t)$) and the boost mode ($V_{\mathrm{src}}^{\mathrm{OC}}(t) < V_{\mathrm{dst}}^{\mathrm{OC}}(t)$), respectively, to further enhance the fitting accuracy.

The high-order curve fitting method is effective in providing approximation of $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ with negligible online computation overhead. The curve fitting results in only 0.02% IME degradation in average when the system is in buck mode compared with the ideal case, i.e., $V_{\mathrm{CTI,opt}}(I_{\mathrm{dst}}(t))$ for given $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$, $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$ and $I_{\mathrm{dst}}(t)$ is given in prior. The IME degradation is 0.15% when the system is in boost mode.

VII. Computation Complexity and Energy Overhead

We compare the online computation complexity among the two optimal solutions proposed in this paper for $S \xrightarrow[[T_0,\infty]]{Q} D$ and $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$, respectively, as well as the near-optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ proposed in [1]. We present the comparison on η_{GME} in Section VIII. We show the computation complexity comparison results in Table IV. In Table IV, N is the number of time slots during the entire charge migration process; M is the number of discrete levels of Q used in Algorithm 1; p is the precision level used in the branch and bound algorithm or the ternary search algorithm. The higher p indicates the higher precision.

TABLE IV
Online Computation Complexity Comparison Among the Three Algorithms

Algorithm		Time complexity
Optimal time-unconstrained	Branch & bound	$O(N \cdot p^2)$
	Ternary search	$O(N \cdot \log^2(p))$
	Lookup table	$O(N)$
Near-optimal time-constrained	Branch & bound	$O(N \cdot p^2)$
	Ternary search	$O(N \cdot \log^2(p))$
	Curve fitting	$O(N)$
Optimal time-constrained	Branch & bound	$O(N \cdot M^2 \cdot p)$
	Ternary search	$O(N \cdot M^2 \cdot \log(p))$
	Curve fitting	$O(N \cdot M^2)$

Table IV shows that we achieve significant online computation complexity reduction through the exploitation of lookup table and high-order curve fitting. We derive the optimal control variable values in $O(1)$ time complexity when equipped with these methods. Moreover, experiments show that $N = 100$ and $M = 200 \sim 400$ will yield good enough charge migration results that are not sensitive to further enhancing the granularity level. In this case, the online computation time for the optimal solution of $S \xrightarrow[[T_0,T_0+T_d]]{Q} D$ is less than 200 ms on a 3.0-GHz desktop computer or less than $1 \sim 2$s on a typical ARM-based embedded processor (as the microcontroller) [16]. Please note that this is the total online computation time of a whole charge migration process, instead of the computation time at a single decision epoch. In conclusion, the optimal solution has reasonable computation complexity for online implementation though its computation complexity is higher than the near-optimal solution.

Next, we discuss about the energy overhead in the microcontroller and peripherals, including current sensors, in the HEES system. We compare the energy overhead with the amount of energy transferred into the destination EES array in a typical charge migration process with 20 V terminal voltage for both source and destination EES arrays, 2-A current flowing into the destination array, and 1000-s migration time. Then the total energy transferred into the destination array is 40 kJ. On the other hand, the power consumption of a typical ARM-based embedded processor is $0.6 \sim 1.2$ W [16], [17]. We know from above that the total online computation time of the microcontroller is less than $1 \sim 2$s for the whole charge migration process of 1000 s, resulting in $0.6 \sim 2.4$ J total energy overhead. For the rest of time, the microcontroller can be power gated or perform optimization for other HEES oper-

TABLE V
COMPARISON OF NORMALIZED GMES IN TIME-UNCONSTRAINED SUPERCAPACITOR-TO-SUPERCAPACITOR CHARGE MIGRATION

T_d	Optimal	Baseline			
			V_{CTI} =1.0V	V_{CTI} =4.5V	V_{CTI} =8.0V
∞	100%	I_{dst} =0.2A	54.6%	69.5%	62.8%
		I_{dst} =0.5A	45.4%	89.2%	86.9%
		I_{dst} =1.0A	30.1%	93.6%	95.6%
		I_{dst} =2.0A	16.6%	85.4%	95.5%
		Adaptive	78.1%	94.9%	99.0%

TABLE VI
COMPARISON OF NORMALIZED GMES IN TIME-UNCONSTRAINED SUPERCAPACITOR-TO-BATTERY CHARGE MIGRATION

T_d	Optimal	Baseline			
			V_{CTI} =3.8V	V_{CTI} =6.9V	V_{CTI} =10.0V
∞	100%	I_{dst} =0.2A	67.3%	57.5%	48.0%
		I_{dst} =0.5A	88.8%	83.7%	75.3%
		I_{dst} =1.0A	97.1%	96.1%	90.4%
		I_{dst} =2.0A	93.8%	98.5%	95.3%
		Adaptive	97.8%	99.2%	95.8%

ations. Hence, the total energy overhead in the microcontroller ($0.6 \sim 2.4$ J) is negligible compared with the amount of energy transferred in a charge migration process (40 kJ). This gap will be even greater for larger-scale HEES systems.

The power dissipation in current sensors associated with each EES array is given by $(I_{\text{src}})^2 \cdot R_{\text{sense}} + (I_{\text{dst}})^2 \cdot R_{\text{sense}}$. In the above charge migration example, the power dissipation in current sensors will be 0.08 W if we assume $R_{\text{sense}} = 10\text{-m}\Omega$ similar to the value in the LTC4000 converter. This power dissipation accounts for only 0.2% of the power transferred into the destination EES array. In general, the sensing overhead in a power system is much less significant compared with that in a digital system due to its much higher power rating.

VIII. EXPERIMENTAL RESULT

This section shows the experimental results of the single-source, single-destination charge migration. We demonstrate the η_{GME} results of all four charge migration scenarios: supercapacitor-to-supercapacitor, supercapacitor-to-battery, battery-to-supercapacitor, and battery-to-battery for both the time-unconstrained and time-constrained charge migrations. We compare the η_{GME} results of the proposed optimal solutions with the baseline systems. We consider two types of baseline systems. Baseline systems of the first type apply constant I_{dst} and V_{CTI} in the charge migration process, independent of time t, whereas the second type applies constant V_{CTI} and optimized $I_{\text{dst}}(t)$ during charge migration. We apply Linear Technology LTM4607 converter as the converter in the HEES system. We extract the parameters required in the converter model (2) and (4) from the datasheet [14]. We obtain characteristics of Li-ion battery by performing measurement on a GP1051L35 Li-ion 2-cell series battery pack with 350-mAh nominal capacity [26] and extracting parameters for the battery model shown in Fig. 3.

A. Time-Unconstrained Charge Migration

We summarize the global migration efficiency η_{GME} results of supercapacitor-to-supercapacitor, supercapacitor-to-battery, battery-to-supercapacitor, and battery-to-battery time-unconstrained charge migrations in Tables V–VIII, respectively. We normalize the η_{GME} values with respect to the results of the optimal solution stated in Section V in each test case. The normalized η_{GME} values of the proposed optimal solution is 100% as annotated with optimal in the tables. The actual η_{GME} values of the optimal solution are

TABLE VII
COMPARISON OF NORMALIZED GMES IN TIME-UNCONSTRAINED BATTERY-TO-SUPERCAPACITOR CHARGE MIGRATION

T_d	Optimal	Baseline			
			V_{CTI} =3.0V	V_{CTI} =5.6V	V_{CTI} =8.2V
∞	100%	I_{dst} =0.2A	67.5%	67.0%	62.4%
		I_{dst} =0.5A	85.9%	89.6%	86.5%
		I_{dst} =1.0A	85.9%	97.2%	96.4%
		I_{dst} =2.0A	65.6%	90.3%	91.6%
		Adaptive	89.0%	98.7%	98.1%

TABLE VIII
COMPARISON OF NORMALIZED GMES IN TIME-UNCONSTRAINED BATTERY-TO-BATTERY CHARGE MIGRATION

T_d	Optimal	Baseline			
			V_{CTI} =7.5V	V_{CTI} =11.9V	V_{CTI} =16.4V
∞	100%	I_{dst} =0.2A	65.3%	60.2%	54.4%
		I_{dst} =0.5A	90.1%	86.4%	81.5%
		I_{dst} =1.0A	99.2%	98.0%	94.7%
		I_{dst} =2.0A	88.7%	90.8%	88.8%
		Adaptive	99.3%	98.1%	95.0%

84.11%, 77.88%, 80.34%, and 78.68%, respectively, in these four cases. The baseline systems of the first type apply constant V_{CTI} and I_{dst} in the charge migration process. The V_{CTI} values in the baseline systems are equal to $V_{\text{src}}^{\text{OC}}(T_0)$, $V_{\text{src}}^{\text{OC}}(T_0) + V_{\text{dst}}^{OC}(T_0)/2$, and $V_{\text{dst}}^{\text{OC}}(T_0)$, respectively. The I_{dst} values are equal to 0.2, 0.5, 1, and 2 A, respectively. The second type of baseline systems applies constant V_{CTI} value and optimized $I_{\text{dst}}(t)$ during charge migration due to potential compliance to standards, compatibility choices, and stability issues. The results of the second type of baseline systems are listed in the rows with the title adaptive. The proposed system and baselines have the same initial conditions and amount of charge to be migrated to the destination array. The initial source and destination supercapacitor array OCVs are given by $V_{\text{src}}^{\text{OC}}(T_0) = 8$ V and $V_{\text{dst}}^{\text{OC}}(T_0) = 1$ V, respectively, and the target migration charge is given by $Q = 1200$ C in the supercapacitor-to-supercapacitor charge migration. We set $V_{\text{src}}^{\text{OC}}(T_0) = 10$ V, $V_{\text{dst}}^{\text{OC}}(T_0) = 3.8$ V (i.e., $V_{\text{SoC}}^{\text{dst}}(T_0) = 0.6$), and $Q = 1000$ C in supercapacitor-to-battery migration. We set $V_{\text{src}}^{\text{OC}}(T_0) = 8.2$ V (i.e., $V_{\text{SoC}}^{\text{src}}(T_0) = 0.9$), $V_{\text{dst}}^{\text{OC}}(T_0) = 3$ V, and $Q = 1000$ C in battery-to-supercapacitor migration. We set $V_{\text{src}}^{\text{OC}}(T_0) = 16.4$ V (i.e., $V_{\text{SoC}}^{\text{src}}(T_0) = 0.9$),

$V_{\rm dst}^{\rm OC}(T_0) = 7.5$ V (i.e., $V_{\rm SoC}^{\rm dst}(T_0) = 0.2$), and $Q = 2000$ C in battery-to-battery migration.

The proposed optimal charge migration control algorithm consistently outperforms the first type of baseline algorithms with constant $I_{\rm dst}$ and $V_{\rm CTI}$, as shown from Table V through Table VIII. Most importantly, because there exists no systematic method determining the optimal constant $I_{\rm dst}$ and $V_{\rm CTI}$ in the baseline systems, it is not surprising for someone to design HEES systems with inappropriate $I_{\rm dst}$ and $V_{\rm CTI}$ in charge migration processes that yield very poor $\eta_{\rm GME}$. The proposed optimal solution shows up to 83.4% enhancement in $\eta_{\rm GME}$ over a poorly configured baseline system. Even the accidentally optimally configured baseline system is up to 4.4% less efficient than the optimal solution. This is because the optimal solution dynamically adjusts $I_{\rm dst}(t)$ and $V_{\rm CTI}(t)$ according to the source and destination EES array SoCs to yield the optimal $\eta_{\rm GME}$. In general, the proposed optimal algorithm achieves more significant efficiency enhancement over the first type of baseline algorithms in supercapacitor-to-supercapacitor charge migration than in battery-to-battery migration. This is because the difference in the optimal $I_{\rm dst}(t)$ at the beginning and at the end of the charge migration process is higher in the former case due to more significant OCV variation in supercapacitor arrays during charge migration.

Comparing with the second type of baseline algorithms, the proposed optimal charge migration control algorithm achieves efficiency enhancement up to 21.9% for a poorly configured $V_{\rm CTI}$ in the baseline system. We can observe that the performance of the second type of baseline algorithms will be close to optimal (0.7% less than the optimal algorithm) under an optimally configured $V_{\rm CTI}$. It also outperforms the first type of baseline algorithms with the same fixed $V_{\rm CTI}$ value by up to 51.5%. We have more observations from the comparison results. First, the proposed optimal charge migration algorithm achieves a relatively low amount of efficiency enhancement over the second type of baseline algorithms in battery-to-battery migration. The reason is that the optimal $V_{\rm CTI}(t)$ value is nearly fixed during the whole battery-to-battery migration process since the OCV of battery arrays changes slowly with SoC. Second, the constant $V_{\rm CTI}$ value will be close-to-optimal if it is set to be in the average of the terminal voltages of the source and destination arrays.

Finally, we analyze the effect of inaccuracy in voltage and current regulation on the charge migration efficiencies. According to the state-of-the-art technologies [14], [15], the voltage regulation inaccuracy is less than 0.5% while the current regulation inaccuracy is less than 1%. We first study the instantaneous migration efficiency degradation of a supercapacitor-to-supercapacitor charge migration at time t with $V_{\rm src}^{\rm OC}(t) = 8$ V and $V_{\rm dst}^{\rm OC}(t) = 1$ V. We assume a worst case 0.5% regulation inaccuracy of $V_{\rm CTI}(t)$ and 1% regulation inaccuracy of $I_{\rm dst}(t)$, and this results in less than 0.02% efficiency degradation. In fact, we need a voltage regulation error of 15% or a current regulation error of 10% to have a 1% instantaneous efficiency degradation, illustrating that the instantaneous efficiency function is quite flat near the optimal value of $I_{\rm dst}(t)$ and $V_{\rm CTI}(t)$. Next, we consider the whole supercapacitor-to-supercapacitor charge migration process with $V_{\rm src}^{\rm OC}(T_0) = 8$ V, $V_{\rm dst}^{\rm OC}(T_0) = 1$ V, and $Q = 1200$ C. We consider that the regulation inaccuracy of $V_{\rm CTI}(t)$ is a uniform distribution between 0% and 0.5% while that of $I_{\rm dst}(t)$ is uniformly distributed between 0% and 1%. Then, the degradation in migration efficiency is less than 0.01% for the whole charge migration process, which is hardly noticeable. Based on these observations, we conclude that the effect of regulation inaccuracy is negligible on charge migration efficiency.

TABLE IX
COMPARISON OF NORMALIZED GMES IN TIME-CONSTRAINED SUPERCAPACITOR-TO-SUPERCAPACITOR CHARGE MIGRATION

T_d (s)	Optimal	Near-opt.	Baseline		
			V_{CTI} =1.0	V_{CTI} =4.5	V_{CTI} =8.0
200	85.4%	76.9%	5.1%	55.8%	69.9%
250	90.9%	85.3%	6.6%	61.8%	74.8%
300	94.0%	90.0%	8.1%	66.3%	78.5%
400	96.9%	94.8%	11.0%	72.8%	89.7%
600	99.4%	99.3%	16.6%	85.4%	95.5%
1,200	100%	100%	30.1%	93.6%	95.6%

TABLE X
COMPARISON OF NORMALIZED GMES IN TIME-CONSTRAINED SUPERCAPACITOR-TO-BATTERY CHARGE MIGRATION

T_d (s)	Optimal	Near-opt.	Baseline		
			V_{CTI} =3.8	V_{CTI} =6.9	V_{CTI} =10.0
200	78.4%	75.8%	54.1%	72.8%	71.1%
300	90.7%	89.2%	76.6%	87.9%	85.9%
400	96.6%	95.5%	87.4%	94.8%	92.2%
600	99.8%	99.7%	96.0%	99.0%	95.1%
1,200	100%	100%	95.9%	93.7%	87.3%

TABLE XI
COMPARISON OF NORMALIZED GMES IN TIME-CONSTRAINED BATTERY-TO-SUPERCAPACITOR CHARGE MIGRATION

T_d (s)	Optimal	Near-opt.	Baseline		
			V_{CTI} =3.0	V_{CTI} =5.6	V_{CTI} =8.2
200	67.3%	N/A	N/A	N/A	N/A
250	75.4%	N/A	N/A	N/A	N/A
300	81.2%	76.9%	N/A	29.6%	73.9%
400	89.2%	88.0%	47.6%	84.5%	86.2%
600	97.3%	96.3%	73.1%	93.7%	94.4%
1,000	100%	100%	85.9%	97.2%	96.4%

B. Time-Constrained Charge Migration

We summarize the global migration efficiency $\eta_{\rm GME}$ results of supercapacitor-to-supercapacitor, supercapacitor-to-battery, battery-to-supercapacitor, and battery-to-battery time-constrained charge migrations in Tables IX–XII, respectively, with T_d shown in the first column of each table. We show the normalized $\eta_{\rm GME}$ values of the optimal solution proposed in Section VI and the near-optimal solution proposed in [1] in the second and third columns, respectively. These values are normalized with respect to the optimal $\eta_{\rm GME}$ in the time-

TABLE XII
COMPARISON OF NORMALIZED GMES IN TIME-CONSTRAINED BATTERY-TO-BATTERY CHARGE MIGRATION

T_d (s)	Optimal	Near-opt.	Baseline		
			V_{CTI} =7.5	V_{CTI} =11.9	V_{CTI} =16.4
600	71.0%	69.9%	63.7%	69.8%	68.9%
1,000	89.9%	89.3%	86.8%	89.3%	87.4%
1,500	98.4%	98.2%	97.2%	97.2%	94.6%
2,000	100%	100%	99.2%	98.0%	94.7%
4,000	100%	100%	90.1%	86.4%	81.5%

unconstrained migration case. The $V_{\text{src}}^{\text{OC}}(T_0)$, $V_{\text{dst}}^{\text{OC}}(T_0)$, and Q values are exactly the same as those used in the time-unconstrained experiments. We only consider the first type of baseline systems with constant V_{CTI} and I_{dst} due to space limitation. We use constant charging current $I_{\text{dst}} = I_{\text{dst,min}}$ in the baseline systems corresponding to the given T_d, in which $I_{\text{dst,min}}$ is defined in [1, eq. (10)]. Charge migration in the baseline systems finishes just before the deadline with the smallest possible constant charging current.

The proposed optimal solution and the near-optimal solution consistently outperform the baseline algorithms under the same deadline constraint, i.e., the same T_d, as illustrated from Table IX through Table XII. The main reason is the flexibility in finding the optimal $I_{\text{dst}}(t)$ and $V_{\text{CTI}}(t)$ that are functions of the source and destination array SoCs. The proposed optimal algorithm outperforms the near-optimal algorithm in two aspects. First, it achieves up to 8.5% in efficiency enhancement compared with the near-optimal algorithm, when the deadline is relatively tight ($T_d = 200$). Please note that this 8.5% efficiency enhancement corresponds to around 21% reduction in energy loss during charge migration, which is significant because charge migration is a frequent operation to enhance the responsiveness and availability of the HEES system. Also, the seemingly small 4.0% efficiency enhancement in supercapacitor-to-supercapacitor migration when $T_d = 300$ corresponds to around 14% reduction in energy loss. There is a second benefit of the optimal solution, as shown in Table XI. When the time constraint is relatively tight, both the near-optimal solution and baselines fail to finish the charge migration. This is because the source battery arrays cannot support the high charging power at the end of charge migration process when the SoC (and terminal voltage) of the destination supercapacitor array becomes high. In this case, only the optimal solution can finish the charge migration process.

To explain the reason that the optimal algorithm outperforms the near-optimal one, Fig. 8 shows as an example the traces of $I_{\text{dst}}(t)$ in the optimal solution and the near-optimal solution of a supercapacitor-to-supercapacitor time-constrained migration when $T_d = 400$. $I_{\text{dst}}(t)$ is higher at the beginning and lower at the end of the charge migration process in the optimal solution using dynamic programming. On the other hand, $I_{\text{dst}}(t)$ is constant during the charge migration process in the near-optimal solution because of the constraint in [1, eq. (11)]. Therefore, the proposed optimal algorithm outperforms the near-optimal algorithm when the deadline is (relatively) tight due to its higher flexibility in choosing the appropriate $I_{\text{dst}}(t)$. Please note that the charging current $I_{\text{dst}}(t)$ at the end of

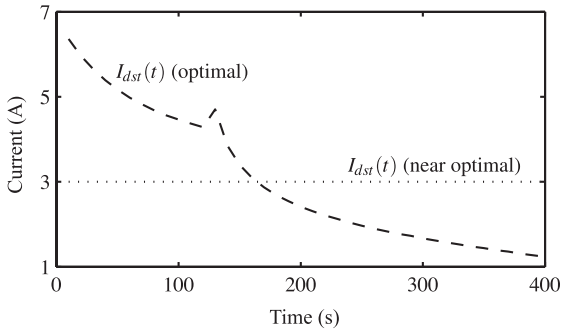


Fig. 8. Traces of $I_{\text{dst}}(t)$ in the optimal solution and near-optimal solution of a time-constrained charge migration.

charge migration process in the optimal solution is lower than that in the near-optimal solution. This explains why the optimal solution does not fail in the battery-to-supercapacitor migration in Table XI because the source battery bank can support the relatively small charging current when the terminal voltage of the destination supercapacitor array becomes high. On the other hand, when the deadline is very loose, the η_{GME} results of both the optimal and the near-optimal solutions converge to the optimal η_{GME} in the time-unconstrained charge migration.

In fact, the energy overhead of microcontroller and peripherals, and the regulation inaccuracy will have very small effect on the 21% reduction in energy loss achieved by the optimal solution, due to the following reasons. First, even when the optimal solution is implemented, the microcontroller energy loss is negligible compared with the energy loss during charge migration as analyzed in Section VII. This is because the microcontroller power consumption (<1.2 W) is much smaller than the power rating of EES arrays (in the order of 50 $\sim$ 100 W), and it can be time-multiplexed to manage other charge management tasks in the HEES system or be simply power gated during idle time. Second, the energy overhead in current sensing, which accounts for about 0.2% of the total energy transferred into the destination array, is the same for the optimal solution and the near-optimal solution. In fact, Coulomb counting is implemented in most state-of-the-art EES systems and therefore is a common overhead. Third, the inaccuracy in voltage or current regulation has negligible effect on the charge migration efficiency. We conclude that the optimal solution of time-constrained charge migration is worthwhile to be implemented when the time constraint is relatively tight, because it can actually reduce a significant portion of energy loss compared with the near-optimal solution and/or increase the chance of success. We would like to point out that it is very common for charge migrations with a tight deadline in HEES operations, because it is often necessary to perform charge migration to enhance the HEES availability for an incoming power profile in the near future or balance the SoCs of various EES arrays.

IX. CONCLUSION

EES systems have a great potential to enhance the power system efficiency. HEES system is one of the most promis-

ing ways to achieve high-performance and low-cost EES systems. This paper introduces the fundamentals of charge migration, which is a key operation in managing the HEES system, including problem definition, formulation, and solution method targeting at the optimal migration efficiency. This paper provides a systematic derivation of the optimal charge migration for the case of a single source and a single destination. We derive the optimal solution for the time-unconstrained charge migration problem. We also derive the optimal solution for the time-constrained charge migration problem based on dynamic programming.

APPENDIX

We have the following two equations from (14) and (15):

$$dV_{\mathrm{SoC}}^{\mathrm{src}}(t) = -\frac{I_{\mathrm{src}}(t)/\eta_{\mathrm{rate,d}}^{\mathrm{src}}(I_{\mathrm{src}}(t))dt}{C_{\mathrm{full}}^{\mathrm{src}}} \tag{28}$$

$$dV_{\mathrm{SoC}}^{\mathrm{dst}}(t) = \frac{I_{\mathrm{dst}}(t)\cdot\eta_{\mathrm{rate,c}}^{\mathrm{dst}}(I_{\mathrm{dst}}(t))dt}{C_{\mathrm{full}}^{\mathrm{dst}}}. \tag{29}$$

Based on the above two equations, we rewrite (16) in the following way:

$$\eta_{\mathrm{GME}} = \frac{C_{\mathrm{full}}^{\mathrm{dst}}\cdot\int_{V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0)}^{V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0+T_d)} V_{\mathrm{dst}}^{\mathrm{OC}}(V_{\mathrm{SoC}}^{\mathrm{dst}}(t))\cdot dV_{\mathrm{SoC}}^{\mathrm{dst}}(t)}{C_{\mathrm{full}}^{\mathrm{src}}\cdot\int_{V_{\mathrm{SoC}}^{\mathrm{src}}(T_0+T_d)}^{V_{\mathrm{SoC}}^{\mathrm{src}}(T_0)} V_{\mathrm{src}}^{\mathrm{OC}}(V_{\mathrm{SoC}}^{\mathrm{src}}(t))\cdot dV_{\mathrm{SoC}}^{\mathrm{src}}(t)} \tag{30}$$

where $V_{\mathrm{dst}}^{\mathrm{OC}}(V_{\mathrm{SoC}}^{\mathrm{dst}}(t))$ is the destination array OCV given SoC $V_{\mathrm{SoC}}^{\mathrm{dst}}(t)$, and $V_{\mathrm{src}}^{\mathrm{OC}}(V_{\mathrm{SoC}}^{\mathrm{src}}(t))$ is the source array OCV given SoC $V_{\mathrm{SoC}}^{\mathrm{src}}(t)$. The nominator of (30) is a constant since both $V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0)$ and $V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0+T_d) = V_{\mathrm{SoC}}^{\mathrm{dst}}(T_0) + Q/C_{\mathrm{full}}^{\mathrm{dst}}$ are constants. Hence, maximizing η_{GME} is equivalent to minimizing the denominator of (30), $C_{\mathrm{full}}^{\mathrm{src}}\cdot\int_{V_{\mathrm{SoC}}^{\mathrm{src}}(T_0+T_d)}^{V_{\mathrm{SoC}}^{\mathrm{src}}(T_0)} V_{\mathrm{src}}^{\mathrm{OC}}(V_{\mathrm{SoC}}^{\mathrm{src}}(t))\cdot dV_{\mathrm{SoC}}^{\mathrm{src}}(t)$. It is furthermore equivalent to maximizing $V_{\mathrm{SoC}}^{\mathrm{src}}(T_0+T_d)$ or minimizing the total amount of charge extracted from the source EES array since $V_{\mathrm{SoC}}^{\mathrm{src}}(T_0)$ is given. We have proved Theorem 1 by far.

REFERENCES

[1] Y. Wang, Y. Kim, Q. Xie, N. Chang, and M. Pedram, "Charge migration efficiency optimization in hybrid electrical energy storage (HEES) systems," in *Proc. IEEE/ACM ISLPED*, Aug. 2011, pp. 103–108.

[2] J. Baker and A. Collinson, "Electrical energy storage at the turn of the millennium," *Power Eng. J.*, vol. 13, no. 3, pp. 107–112, Jun. 1999.

[3] D. H. Doughty, P. C. Butler, A. A. Akhil, N. H. Clark, and J. D. Boyes, "Batteries for large-scale stationary electrical energy storage," *Electrochem. Soc. Inter.*, vol. 19, no. 3, pp. 49–53, 2010.

[4] H. T. Odum, "Energy quality and carrying capacity of the earth," *Tropical Ecol.*, vol. 16, no. 1, pp. 1–8, 1975.

[5] C. J. Cleveland, "Energy quality and energy surplus in the extraction of fossil fuels in the U.S.," *Ecol. Econom.*, vol. 6, no. 2, pp. 139–162, Oct. 1992.

[6] H. Chen, T. N. Cong, W. Yang, C. Tan, Y. Li, and Y. Ding, "Progress in electrical energy storage system: A critical review," *Progr. Natural Sci.*, vol. 19, no. 3, pp. 291–312, Mar. 2009.

[7] M. Pedram, N. Chang, Y. Kim, and Y. Wang, "Hybrid electrical energy storage systems," in *Proc. 16th ACM/IEEE ISLPED*, Aug. 2010, pp. 363–368.

[8] F. Koushanfar and A. Mirhoseini, "Hybrid heterogeneous energy supply networks," in *Proc. IEEE ISCAS*, May 2011, pp. 2489–2492.

[9] Q. Xie, Y. Wang, Y. Kim, N. Chang, and M. Pedram, "Charge allocation for hybrid electrical energy storage systems," in *Proc. 9th IEEE/ACM/IFIP CODES+ISSS*, Oct. 2011, pp. 277–284.

[10] Y. Kim, S. Park, Y. Wang, Q. Xie, N. Chang, M. Poncino, *et al.*, "Balanced reconfiguration of storage banks in a hybrid electrical energy storage system," in *Proc. ICCAD*, 2011, pp. 1–8.

[11] Q. Xie, Y. Wang, Y. Kim, D. Shin, N. Chang, and M. Pedram, "Charge replacement in hybrid electrical energy storage systems," in *Proc. 17th ASP-DAC*, Feb. 2012, pp. 627–632.

[12] Y. Wang, Q. Xie, M. Pedram, Y. Kim, N. Chang, and M. Poncino, "Multiple-source and multiple-destination charge migration in hybrid electrical energy storage systems," in *Proc. DATE*, Mar. 2012, pp. 169–174.

[13] Y. Kim, S. Park, Q. Xie, Y. Wang, N. Chang, and M. Pedram, "Networked architecture for hybrid electrical energy storage systems," in *Proc. 49th ACM/EDAC/IEEE DAC*, Jun. 2012, pp. 522–528.

[14] *LTM4607: 36 V in, 24 V Out High Efficiency Buck-Boost DC/DC MicroModule*, Linear Technology, Milpitas, CA, USA, 2008.

[15] *LTC4000: High Voltage High Current Controller for Battery Charging and Power Management*, Linear Technology, Milpitas, CA, USA, 2008.

[16] *Samsung Exynos 4 Dual 45nm (Exynos 4210) RISC Microprocessor*, Samsung Group, Seoul, Korea, 2012.

[17] *Texas Instruments LM3S2965 Stellaris LM3S Microcontroller*, Texas Instruments Inc., Dallas, TX, USA, 2010.

[18] Y. Choi, N. Chang, and T. Kim, "DC–DC converter-aware power management for low-power embedded systems," *IEEE Trans. Comput., Aided Des. Integr. Circuits Syst.*, vol. 26, no. 8, pp. 1367–1381, Aug. 2007.

[19] P. Rong and M. Pedram, "An analytical model for predicting the remaining battery capacity of lithium-ion batteries," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 5, pp. 441–451, May 2006.

[20] D. Rakhmatov, "Battery voltage modeling for portable systems," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 14, no. 2, pp. 1–36, Mar. 2009.

[21] M. Chen and G. Rincon-Mora, "Accurate electrical battery model capable of predicting runtime and I-V performance," *IEEE Trans. Energy Convers.*, vol. 21, no. 2, pp. 504–511, Jun. 2006.

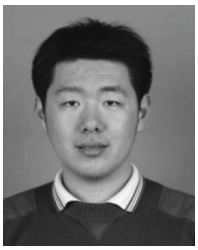
[22] D. Shin, Y. Wang, Y. Kim, J. Seo, N. Chang, and M. Pedram, "Battery-supercapacitor hybrid system for high-rate pulsed load applications," in *Proc. DATE*, Mar. 2011, pp. 1–4.

[23] D. Linden and T. B. Reddy, *Handbook of Batteries*. New York, NY, USA: McGraw-Hill, 2001.

[24] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein, *Introduction to Algorithms*, 3rd ed. Cambridge, MA, USA: MIT Press, 2009.

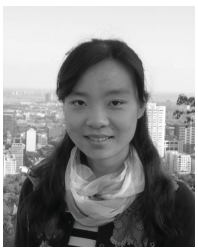
[25] C. M. Bishop, *Pattern Recognition and Machine Learning*. New York, NY, USA: Springer-Verlag, 2006.

[26] *GP Batteries Datasheet: Model GP1051L35*, Gold Peak Industries, San Diego, CA, USA, 2011.



Yanzhi Wang (S'12) received the B.S. (Hons.) degree in electronic engineering from Tsinghua University, Beijing, China, in 2009. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Southern California, Los Angeles, CA, USA, under the supervision of Prof. M. Pedram.

He has published over 75 papers. His current research interests include system level power management, next-generation energy sources, hybrid electrical energy storage systems, near-threshold computing, cloud computing, mobile devices, and smart grid.



Xue Lin (S'12) received the B.S. degree from Tsinghua University, Beijing, China, in 2009. She is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA, under the supervision of Prof. M. Pedram.

She is involved in power management of photovoltaic systems, near-threshold computing of FinFET circuits, and power management of energy storage systems. She has published over 25 papers.

Younghyun Kim (M'13) received the B.S. (Hons.) degree in computer science and engineering and the Ph.D. degree in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2007 and 2013, respectively.

He was a Visiting Scholar with the University of Southern California, Los Angeles, CA, USA, from 2009 to 2011. He is currently a Post-Doctoral Research Assistant with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA. His current research interests include secure medical devices, system-level power management, energy harvesting, and storage systems.

Dr. Kim was the winner of the ISLPED Low Power Design Contest in 2007 and 2012, and received the IEEE SSCS Seoul Chapter Best Paper Award in ISOCC in 2009.

Qing Xie (S'12) received the B.S. and M.S. degrees in physics from Fudan University, Shanghai, China, in 2007, and Northeastern University, Boston, MA, USA, in 2009. He is currently pursuing the Ph.D. degree from the Electrical Engineering Department, University of Southern California, Los Angeles, CA, USA, under the supervision of Prof. M. Pedram.

His current research interests include low-power systems design, energy storage systems, system-level power management, thermal management, and near threshold computing.

Mr. Xie has received the Best Paper Award from the 30th IEEE International Conference on Computer Design.

Massoud Pedram (F'01) received the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1991.

He is the Stephen and Etta Varra Professor with the Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA. He holds ten U.S. patents and has published four books, 12 book chapters, and more than 130 archival and 340 conference papers. His current research interests include low power electronics, energy-efficient processing, cloud computing to photovoltaic cell power generation, energy storage, power conversion, RT-level optimization of VLSI circuits to synthesis, and physical design of quantum circuits.

Dr. Pedram received six conference and two IEEE Transactions Best Paper Awards. He is a recipient of the 1996 Presidential Early Career Award for Scientists and Engineers, an ACM Distinguished Scientist, and currently serves as the Editor-in-Chief of the *ACM Transactions on Design Automation of Electronic Systems* and the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS. He has served on the technical program committee of a number of premiere conferences and was the Founding Technical Program Co-Chair of the 1996 International Symposium on Low Power Electronics and Design and the Technical Program Chair of the 2002 International Symposium on Physical Design.

Naehyuck Chang (F'12) received the B.S., M.S., and Ph.D. degrees from the Department of Control and Instrumentation, Seoul National University, Seoul, Korea, in 1989, 1992, and 1996, respectively.

He joined the Department of Computer Engineering, Seoul National University, in 1997, and is currently a Professor with Department of Electrical Engineering and Computer Science, Seoul National University, and the Vice Dean of the College of Engineering, Seoul National University. His current research interests include low-power embedded systems, hybrid electrical energy storage systems, and next-generation energy sources.

Dr. Chang serves on the technical program committees in many EDA conferences, including DAC, ICCAD, ISLPED, DATE, CODES+ISSS, and ASP-DAC. He was a TPC Co-Chair of RTCSA in 2007, ISLPED in 2009, ESTIMedia in 2009 and 2010, and CODES+ISSS in 2012, and is serving as a TPC Chair of ICCD in 2014 and ASP-DAC in 2015. He was the General Vice-Chair of ISLPED in 2010, and a General Chair of ISLPED in 2011 and ESTIMedia in 2011. He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, the *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, the *ACM Transactions on Embedded Computing Systems (TECS)*, and the *Springer Design Automation for Embedded Systems* and was a Guest Editor of ACM TODAES in 2010 and ACM TECS in 2010 and 2011. He is the ACM SIGDA Chair and an ACM Distinguished Scientist.