Performance Prediction for Multiple-Threshold 7nm-FinFET-Based Circuits Operating in Multiple Voltage Regimes Using a Cross-Layer Simulation Framework

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Abstract

Because of their many attractive attributes, FinFETs are emerging as the device of choice for CMOS process technology nodes below 20nm. This paper is the first work that investigates the effectiveness of building CMOS circuits operating in the near-threshold regime and above with 7nm FinFET technology through a cross-layer design and simulation framework. Three types of FinFET devices with different threshold voltages are designed using Sentaurus TCAD to accommodate the need for constructing both high-speed cells and low-power cells in the same library. Compact and SPICE-compatible device models are extracted with high accuracy using current source modeling techniques. Standard cell libraries with two different (near- and super-threshold) supply voltages are generated. Circuit syntheses are performed on extensive benchmarks to compare the performance with the state-of-the-art planar CMOS counterparts. Simulation results demonstrate the benefit of 7nm FinFET-based circuits from both aspects of speed and energy efficiency.

Keywords: FinFET, near-threshold computing, multiple-threshold devices, cross-layer simulation, current source modeling, energy consumption

Introduction

As the geometric dimension of transistors scales down, FinFET devices are proved to better address the challenges facing conventional planar CMOS devices, e.g. high leakage power dissipation, significant short channel effect, etc [1]. Due to manufacturing limitations, deeply scaled FinFET devices below 10nm feature size have not been manufactured. Nevertheless, it is crucial to investigate the performance of such devices with lower feature sizes in order to shed some light on further studies on novel process techniques and circuit structures. A well-known predictive FinFET model, PTM-MG [2], which is based on the BSIM-MG model [3], have been proposed. In this paper, we present an alternative method based on TCAD device simulation and the *current source modeling* (CSM) technique to design and characterize FinFET devices with different threshold voltages, which is believed to be more accurate. Besides, this paper for the first time presents a cross-layer design and simulation framework in which the performance of 7nm-FinFET-based circuits is evaluated in both the near- and super-threshold regimes.

Framework Overview

As shown in Fig. 1, the proposed design framework is mainly comprised of three parts, i.e. (1) FinFET device modeling and design, (2) compact and SPICE-compatible device model extraction, and (3) standard cell library construction and circuit synthesis results.

A. FinFET Device Modeling and Design

We model and simulate 7nm FinFET devices using Sentaurus TCAD tools [4]. The device model is shown in Fig. 2. To mitigate the direct source-to-drain tunneling (DSDT) current [5], the gate underlap is introduced. It is worth noting that the designs of both nfets and pfets have three versions with different threshold voltages that vary in the range between 0.20V and 0.45V. The design with the lowest V_{th} can be used on the critical path(s) of a circuit for high speed operation, while the designs with higher V_{th}'s can be used on the non-critical paths in order to reduce power dissipation. The three different V_{th}'s are achieved by tuning the gate workfunction of the devices. Table I shows the design parameters.

The Sentaurus device simulations apply the hydrodynamic carrier transport model, Oldslotboom bandgap narrowing model, and the density gradient quantization correction model. The carrier mobility degradation resulting from high doping, high field saturation, and scattering at silicon-insulator interfaces is also taken into account.

B. Compact Model Extraction

We extract the compact models of FinFET devices using the CSM technique, in which an nfet or pfet is modeled as a set of current sources and parasitic capacitances. In this paper, we only consider the case in which the front gate and the back gate of a fin are tied together, with the corresponding current source model shown in Fig. 3. The terminal voltage dependent output currents and capacitance values are characterized by performing proper DC and/or transient terminal voltage sweepings similar to the method described in [6]. And finally, similar to [7], we import the extracted parameters into lookup-table-based Verilog-A models that are SPICE-compatible, for the convenience of further circuit level simulations.

C. Standard Cell Library Construction and Circuit Synthesis

We build up the standard cell libraries in an industrial standard format, the Liberty library format (.lib), in which logic cells, either combinational or sequential, are modeled by recording the timing and power parameters under a specific supply voltage and process technology. The standard cell library can be used to synthesize arbitrary digital circuits using Synopsys Design Compiler. In this paper, we consider both the near-threshold and super-threshold computing scenarios for the multi-threshold FinFET devices, which have the supply voltage of 0.3V and 0.45V, respectively. The timing and power parameters are obtained through HSPICE simulations based on the Verilog-A models under different input and output conditions.

Results and Discussion

Fig. 4 and Fig. 5 show the I_d-V_g curves and the I_d-V_d curves of three types of designs of nfets. Nfet 1 has the lowest threshold voltage, Nfet 3 has the highest threshold voltage, and Nfet 2 has a threshold voltage between the other two. For all three types of designs, the subthreshold slope is ~80mV/dec. When $V_d = V_g = 0.5$V, the drain current of Nfet 1 is 1.8x larger than Nfet 2 and 6.7x larger than Nfet 3.

Fig. 6 shows the minimum energy point (MEP) and minimum energy-delay product point (MEDP) of the FinFET designs with three different threshold voltages. We test a 20-stage inverter chain with varying activity factors. As shown in Fig. 6, the MEP lies around 0.2V, which is in the subthreshold regime, whereas the MEDP begins to occur in the near-threshold regime.

Table II shows the delay and power consumption comparison in a number of benchmark circuits using the synthesis results of our 7nm FinFET-based cell library with OSU 45nm CMOS standard cell library and NANGATE 45nm CMOS cell library as baselines. Comparing the low-threshold 7nm FinFET cell library at 0.3V with the OSU 45nm CMOS standard cell library (operating at 1.1V), we achieve a maximum of 8.7x reduction in circuit delay/clock period and maximum of 1400x reduction in energy per operation.

Conclusion

This paper provided a 7nm FinFET standard cell library for HSPICE simulations based on device models built in Sentaurus TCAD. The simulations run on some benchmarks show significant improvement in terms of delay and energy consumption when using FinFETs instead of planar CMOS devices.

References

[1] L. Chang, *et al*, *Proc. of the IEEE*, 2003. [2]S. Sinha, *et al*, *Proc. DAC*, 2012. [3] M. V. Dunga, *et al*, *VLSIT*, 2003. [4] [Online] http://www.synopsys.com/tools/tcad/. [5] R. A. Vega, *et al*, *IEEE TED*, 2009. [6] H. Fatemi, *et al*, *Proc. DAC*, 2006. [7] A. A. Goud, *et al*, *DRC*, 2013.

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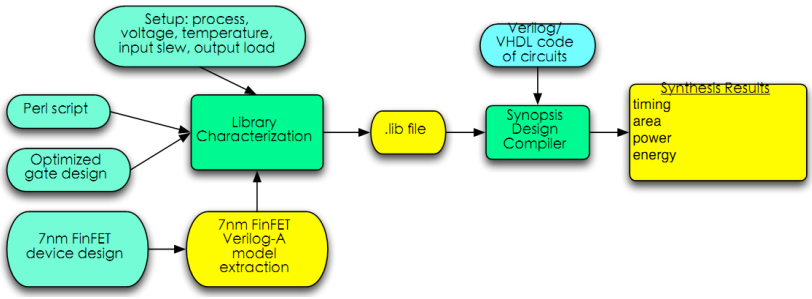

Fig 1. An overview of the proposed cross-layer design and simulation framework of 7nm FinFET devices and circuits. The three major steps are:

(1) FinFET device design and modeling;
(2) SPICE-compatible compact model extraction;
(3) Standard cell library construction and circuit synthesis.

TABLE I
FINFET DESIGN PARAMETERS

Parameter Name	Value
Gate Length	7nm
Gate Width	3.5nm
Gate Height	14nm
Gate Oxide Material	$HfO_2 + SiO_2$
Gate Oxide Thickness	1.3nm
Gate Underlap	1.5nm on each side
Source/Drain Doping	$1\times10^{20}cm^{-3}$
Nfet Gate Workfunction	4.4eV ~ 4.6eV
Pfet Gate Workfunction	4.7eV ~ 4.9eV

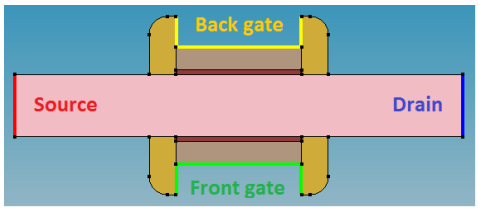

Fig.2 FinFET device model in TCAD tools

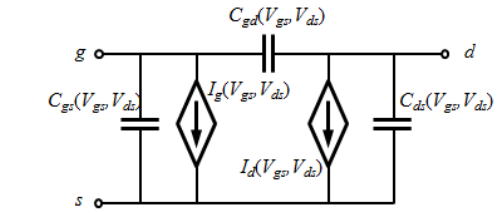

Fig. 3 Current source model for a FinFET transistor. The output currents of the current source and the values of the parasitic capacitances are all functions of voltage pair (V_{gs}, V_{ds}).

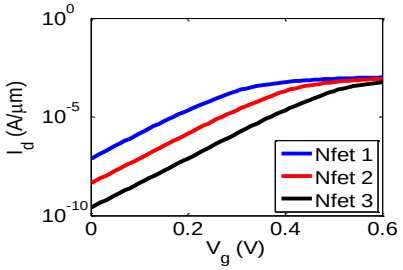

Fig. 4 I_d - V_g curves of three different designs of nfets with different threshold voltages when $V_d = 0.1$V

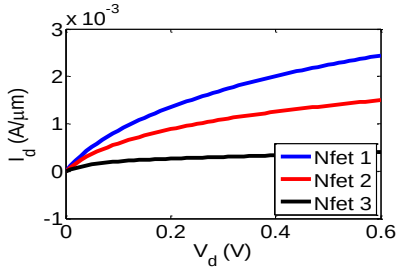

Fig. 5 I_d - V_d curves of three different designs of nfets with different threshold voltages when $V_g = 0.5$V

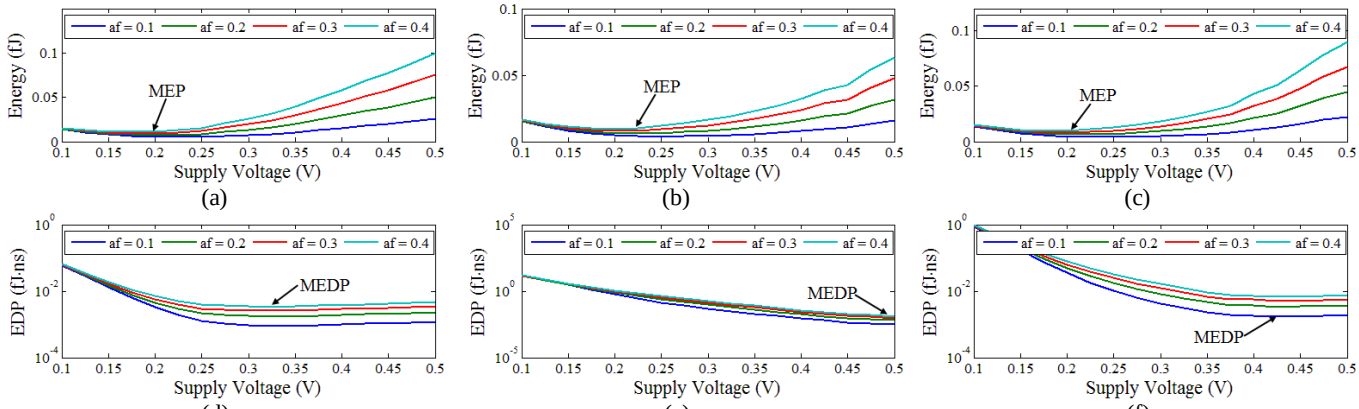

Fig. 6 (a) ~ (c) are the Energy-Supply voltage curves under different activity factors, ranging from 0.1 to 0.4, obtained from a 20-stage inverter chain built from the low-, high-, and medium-V_{th} FinFETs. (d) ~ (f) are the Energy delay product-Supply voltage curves under different activity factors of the same set of FinFET devices. The MEPs and MEDPs are marked in the figure. All MEPs are in the subthreshold region. MEDPs begin to occur in the near-threshold regime.

TABLE II BENCHMARK CIRCUIT PERFORMANCE ON OUR CELL LIBRARY AND 45NM CMOS STANDARD CELL LIBRARIES
(a) ISCAS benchmark circuit C499; (b) ISCAS benchmark circuit C3540; (c) 16-bit adder; (d) 16-bit multiplier

Cell Library	Delay (ns)	Energy per Operation (J)	Cell Library	Delay (ns)	Energy per Operation (J)	Cell Library	Delay (ns)	Energy per Operation (J)	Cell Library	Delay (ns)	Energy per Operation (J)
Lib1	0.100	1.7507e-15	Lib1	0.130	3.44e-15	Lib1	0.150	407.86e-18	Lib1	0.350	6.67e-15
Lib2	7.500	1.2500e-15	Lib2	11.20	1.96e-15	Lib2	10.00	246.62e-18	Lib2	25.00	4.57e-15
Lib3	0.800	741.51e-18	Lib3	1.000	2.00e-15	Lib3	0.700	349.40e-18	Lib3	2.000	5.74e-15
Lib4	0.080	3.1732e-15	Lib4	0.100	6.44e-15	Lib4	0.070	1.3700e-15	Lib4	0.200	22.6e-15
Lib5	0.300	2.6187e-15	Lib5	0.400	5.77e-15	Lib5	0.300	895.73e-18	Lib5	0.800	14.7e-15
Lib6	0.100	3.0896e-15	Lib6	0.130	7.12e-15	Lib6	0.100	1.3819e-15	Lib6	0.350	19.4e-15
Base1	0.600	997.28e-15	Base1	1.500	2.39e-12	Base1	1.310	219.79e-15	Base1	2.710	6.30e-12
Base2	0.600	590.36e-15	Base2	1.500	1.18e-12	Base2	1.450	102.48e-15	Base2	2.890	3.30e-12
(a)			(b)			(c)			(d)		

Lib1 ~ Lib3 are cell libraries obtained under supply voltage of 0.3V with low-, high-, and medium-V_{th} FinFETs, respectively. Lib4 ~ Lib6 are cell libraries obtained under supply voltage of 0.45V with low-, high-, and medium-V_{th} FinFETs, respectively. Base1 is OSU 45nm CMOS standard cell library, and Base2 is NANGATE 45nm CMOS standard cell library. Base1 and Base2 operate at 1.1V supply voltage.