NBTI-Aware Flip-Flop Characterization and Design

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ABSTRACT

With the scaling down of the CMOS technologies, Negative Bias Temperature Instability (NBTI) has become a major concern due to its impact on PMOS transistor aging process and the corresponding reduction in the long-term reliability of CMOS circuits. This paper investigates the effect of NBTI phenomenon on the setup and hold times of flip-flops. First, it is shown that NBTI tightens the setup and hold timing constraints imposed on the flip-flops in the design. Second, different types of flip-flops exhibit different levels of susceptibility to NBTI-induced change in their setup/hold time values. Finally, an NBTI-aware transistor sizing technique can minimize the NBTI effect on timing characteristics of the flip-flops.

Categories and Subject Descriptors: B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids.

General Terms*:* Performance, Design, Reliability.

Keywords: Static timing analysis, setup and hold times, NBTI, circuit reliability, device aging.

1. INTRODUCTION

As CMOS transistors are scaled toward ultra deep submicron technologies, circuit reliability cannot be ignored. Device aging processes such as the Negative Bias Temperature Instability (NBTI) can have a huge impact on the circuit performance over time. Indeed the NBTI effect has proven to be a rising threat to the circuit reliability in nanometer scale technology. Due to NBTI effect, the threshold voltage of the PMOS transistors increases over time, resulting in reduced switching speeds for logic gates, and the corresponding degradation in circuit performance and increased probability of circuit failure due to timing constraint violations [1][2].

NBTI effect is created by trap generation at the Si/SiO_2 interface in PMOS transistors under the negative bias condition ($V_{GS} = -V_{DD}$) at elevated temperatures and degrades the device driving current. The interaction of inversion layer holes with hydrogen passivated Si atoms can break the Si-H bonds, creating an interface trap and one H atom that can diffuse away from the interface or can anneal an existing trap [1]. However, with time, these Si-H bonds can easily break during operation (i.e., ON-state, negative gate bias for the PMOS). The broken bonds act as interfacial traps and increase the threshold voltage of the device, thus affecting the performance of the integrated circuit. NBTI impact gets more severe in scaled technology due to higher die temperatures and utilization of ultra thin gate oxide [5].

The effect of NBTI on digital CMOS circuit performance has been methodically studied in [1][6]. Recently, techniques have been proposed to alleviate the temporal degradation of the CMOS circuit performance. In [5], for example, it was shown that the performance degradation of the CMOS circuit can be offset by cell-level up-sizing during the initial design to compensate for the NBTI-induced decrease in speed of the PMOS device a priori. The authors of [9] showed that the NBTI degradation in memory circuits can increase the failure rate of the system and proposed a circuit technique to address the problem.

Although these works address the NBTI effect on circuit performance, none has considered the effect of NBTI on the setup/hold time characteristic of the sequential circuit elements (i.e., latches and flip-flops). In [10] it was stated that in the presence of NBTI, the setup and hold time of the flip-flops remain nearly constant. In this paper, however, we show that setup and hold times of flip-flops change due to NBTI and the codependency between them tightens timing constraints over time.

Operating frequencies of more than 1 GHz are common in modern integrated circuits. As the clock period decreases, inaccuracy in setup/hold times caused by corner-based static timing analysis (STA) tools becomes less acceptable. Optimism in setup/hold time calculation can result in circuit failure, while pessimism leads to inferior performance [4]. Therefore, accurate characterization of the setup and hold times of latches and registers is critically important for timing analysis of digital circuits [7]. Setup and hold times are co-dependent [4] in the sense that there are multiple pairs of setup and hold times that result same clock-to-q. All pairs of setup/hold times that correspond to a constant clock-to-q delay are placed on a contour of clock-to-q delay surface. Salman et al. in [4] presented a methodology to co-dependently characterize the setup and hold times of sequential circuit elements (SCE's) and used the resulting multiple pairs in STA. An Euler-Newton curve tracing procedure was proposed in [7] and [8] to efficiently characterize the setup and hold times codependency. The codependent setup/hold contours are utilized to evaluate setup and hold slacks.

In this paper we show how the NBTI effect alters the setup/hold time codependency characterization. We define a criterion to quantify the NBTI effect for different flip-flops. We also show how to size the transistors of a flip-flop to minimize the NBTI effect on its timing characteristics while incurring minimum hardware and power consumption overhead.

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The remainder of the paper is organized as follows. Section 2 provides some background on NBTI effect and flip-flop characterization. It also defines the terminology which will be used in subsequent sections. The effect of NBTI on Co-dependent Setup/Hold Time (CSHT) characterization is described in Section 3. NBTI-aware flip-flop design to minimize the NBTI effect is discussed in Section 4. Section 5 gives the simulation results and Section 6 concludes the paper.

2. BACKGROUND

This section provides the terminology, reviews the manifestation of NBTI on threshold voltage of a PMOS transistor, the CSHT characteristic contour for a given clock-to-q delay, and explains how to utilize this contour in a STA tool for timing verification.

2.1 Technology

All results presented in this paper are obtained by HSPICE [14] simulations using a predictive 130nm technology model [13] with 1.2V for the supply voltage and 0.35V for the nominal threshold voltage.

2.2 NBTI Effect

The recent aggressive scaling of CMOS technology makes NBTI one of the dominant reliability concerns in nanoscale designs [3]. It is believed that NBTI is caused by broken Si-H bonds, which are induced by positive holes from the channel. Then H, in a neutral form, diffuses away; positive traps are left, which cause the increase of voltage threshold of the PMOS transistors [11].

For a PMOS transistor, there are two phases of NBTI, depending on its bias condition. In phase I, when V_G=0 (i.e., V_{GS}= –V_{DD}), positive interface traps are accumulating during the stress time with H atoms diffusing towards the gate. This phase is usually referred to as "stress" or "static NBTI". In phase II, when V_G=V_{DD} (i.e., V_{GS}=0), holes are not present in the channel, and thus, no new interface traps are generated; instead, H atoms diffuse back and anneal the broken Si-H. As a result, the number of interface traps is reduced during this stage and some of the NBTI effect is reversed. Phase II is referred to as "recovery" and can have a significant impact on NBTI effect estimation in VLSI circuits. The stress and recovery phases together are called "dynamic NBTI". See, for example, reference [12] for a plot of successive rise and fall in the magnitude of V_{th} of a PMOS transistor during repeated stress and recovery phases.

In this paper, we consider the circuit under dynamic NBTI to model realistic circuit operation. There are some analytical models to express the change in V_{th} under dynamic NBTI [1][6][11]. In this paper in order to predict the threshold voltage degradation due to the NBTI effect at a time t and also considering duty cycle of stress vs. recovery phases, we adopt the model of reference [6].

2.3 Codependent Setup and Hold Time

Latches and flip-flops are sequential circuit elements used in synchronous designs where a clock edge is used to sample and store a logic value on a data line. The **setup time,** τ_s, is the *minimum time before* the active edge of the clock that the input data line must be valid for reliable latching. Similarly, the **hold time**, τ_h, represents the *minimum time* that the data input must be held stable *after* the active clock edge. The active clock edge is the transition edge (either low-to-high or high-to-low) at which data transfer/latching occurs. The **clock-to-q** delay refers to the propagation delay from the 50% transition of the active clock edge to the 50% transition of the output, q, of the latch/register. The s**etup skew** refers to the delay from the latest 50% transition edge of the data signal to the 50% active clock transition edge; similarly, the **hold skew** denotes the delay from the 50% active clock transition edge to the earliest 50% transition edge of the data signal. Figure 1 illustrates the setup and hold skews, which are denoted by τ_{sw} and τ_{hw}, respectively.

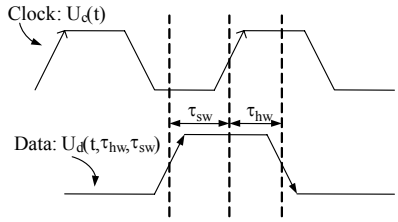

Figure 1. Setup and hold skews shown on the data and clock waveforms.

A common technique for setup/hold time characterization is to plot the clock-to-q delay for various setup and hold skews via a series of transient simulations. This process in turn produces a clock-to-q *delay surface*. The setup (hold) time is then taken as a particular setup (hold) skew point on the plot, for which the *characteristic clock-to-q*[1], t_{cc2q}, delay increases by say 10%. (We shall denote as t_{c2q} the clock-to-q delay which is 10% higher than t_{cc2q}.) The setup (hold) time is typically made more accurate by identifying an interval around the initial estimate of the setup (hold) time and running transient simulations in that interval according to a binary search method.

As already noted, the setup and hold times are not independent quantities, but depend strongly on one another. Typically, the setup time decreases as the hold skew increases and vice versa. Similarly, the hold time decreases as the setup skew increases and vice versa. The tradeoff between setup and hold skews and the hold and setup times is a strong function of the flip-flop design.

A general method to extract codependent pairs of setup/hold times is to first obtain the clock-to-q surface. This is followed by extraction of a contour in the setup/hold time plane that contains all points that result in a given increase (*e.g.*, 10% is typical) in t_{cc2q}. Figure 2 (a) and (b) show a typical clock-to-q surface and a CSHT contour plot. Figure 2 (c) depicts that setup and hold time pairs decrease when clock-to-q increases.

2.4 Setup and Hold Slacks and Required Times

In general, a STA tool reads in a circuit netlist, a cell library, and a clock period T [4]. The tool reports whether new data values can be introduced in a (pipelined) circuit every T seconds. This analysis is accomplished by computing the worst **setup slack** (s_s) and the worst **hold slack** (s_h) for any flip-flop in the circuit. Referring to Figure 3, these slacks are computed as follows:

$$s_s \equiv \min(\tau_{sw}) - \tau_s = T + \min(D_{p2}) - t_{c2q} - \max(D_{p1} + D_c) - \tau_s \quad (1)$$

$$s_h \equiv \min(\tau_{hw}) - \tau_h = t_{c2q} + \min(D_{p1} + D_c) - \max(D_{p2}) - \tau_h \quad (2)$$

[1] If the setup skew is larger than a certain value, then the clock-to-q delay of a flip-flop will become independent of the setup skew; this constant clock-to-q delay which is achieved for large setup skews is called the "characteristic clock-to-output delay" of the flip-flop.

where D_{p1}, D_{p2}, and D_c stand for the delays of local clock signals compared to the global clock, and delay of the combinational logic encased between the input and output flip-flops, respectively as illustrated in Figure 3.

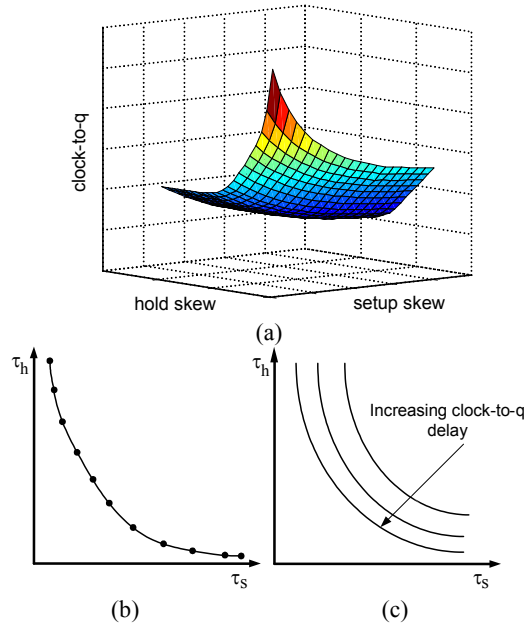

Figure 2. (a) A clock-to-q surface, (b) A setup/hold time contour, (c) setup/hold time contours with different clock-to-q values.

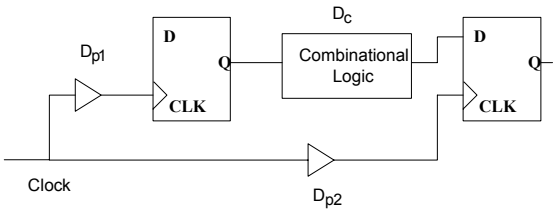

Figure 3. Definition of s_s and s_h in a synchronous data path.

If a slack is negative, it is said to be "violated". If a setup slack, s_s, is violated, the circuit can operate correctly only by increasing T. If a hold time, s_h, is negative, the circuit will not function correctly unless delay elements are inserted on the short paths in the combinational logic.

The **required setup time** (RST) for a given flip-flop is defined as the minimum value of τ_{sw} for that flip-flop which results in a non-negative setup slack (i.e., the minimum setup skew needed to eliminate setup time violations for the flip-flop). The **required hold time** (RHT) is defined similarly. On the other hand, the area above the CSHT contour is a pessimistic area where the flip-flop can correctly work in while the area under the CSHT contour is an overly optimistic area. Optimism is not permissible in STA, because it may result in failing chips. Therefore, the feasible working area for the flip-flop is the area above the CSHT contour. In addition, RST and RHT constraints must be satisfied. Hence, the flip-flop should be designed in a way to work in the shaded region in Figure 4 which is called the *Feasible Region* (FR).

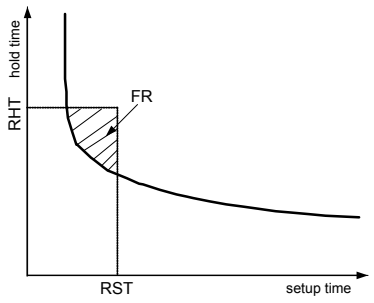

Figure 4. RST, RHT and FR in CSHT contour.

3. NBTI EFFECT AND CSHT CHARACTERIZATION

Increasing the threshold voltage of PMOS transistors, due to NBTI effect, results in variation in the CSHT characteristics. This means that for the same t_{c2q}, a new set of setup/hold time pairs should be obtained (cf. Figure 5 for a pictorial explanation). On the other hand, due to the NBTI effect, delay of combinational circuits itself increases. Therefore, given a fixed clock frequency, RST and RHT values will change and new STA requirements should be specified to achieve timing closure. By using NBTI-aware design techniques [5] the delay of combinational logic blocks and clock drivers can be kept relatively unchanged. Furthermore, we shall use the original (NBTI-unaffected) t_{c2q} value for computing the new CSHT contours. Therefore, the RST and RHT values do not change due to the NBTI effect. Notice that it is possible to extend our methodology to handle changes in the RST and RHT values.

In the presence of NBTI effect, a timing failure occurs when the new CSHT contour has no intersection with the FR. This means there is no setup and hold time pairs that result in non-negative setup and hold slacks. Figure 5 illustrates the effect of NBTI on the CSHT for the timing failure and non-failure cases.

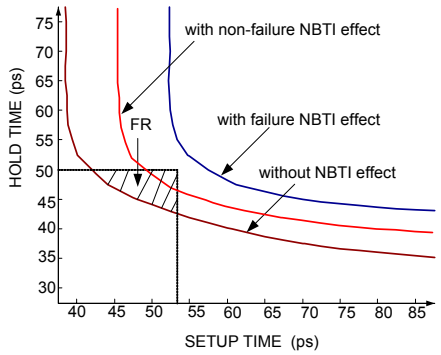

Figure 5. Setup/hold time codependency change due to the NBTI effect.

3.1 Critical Pairs Definition for NBTI

As discussed in the previous section, setup and hold time contours change due to the NBTI effect. This change is, however, different from one flip-flop type to the next. We define a measure to calculate this change. The measure has to contain the movement of the CSHT curve in the direction of x (setup time) and y (hold time) axes for the same t_{c2q}. To define this measure, first we introduce two critical pairs on the setup and hold time contour.

Definition 1: Γ is defined as the set of all (τ_s, τ_h) pairs on a CSHT contour.

Definition 2: The *setup lower bound* (SLB) is defined as τ_s when $\tau_h \to \infty$.

Definition 3: The *hold lower bound* (HLB) is defined as τ_h when $\tau_s \to \infty$.

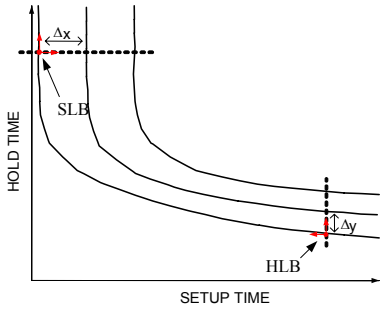

Figure 6. Different contours Γ corresponding to different aging.

Definition 4: Assume Γ^{NBTI} is the CSHT contour after NBTI effect. The movement of the SLB and HLB in *x* (setup time) and *y* (hold time) directions with respect to original contour Γ are denoted by Δx_{SLB} and Δy_{HLB}, respectively. The setup and hold time growth (SHG) is defined as the maximum of the summation of percentage movements in SLB and HLB for a rising or falling output transition:

$$SHG = \frac{\max\left(\Delta x_{SLB,r}, \Delta x_{SLB,f}, 0\right)}{x_{SLB}} + \frac{\max\left(\Delta y_{HLB,r}, \Delta y_{HLB,f}, 0\right)}{y_{HLB}} \quad (3)$$

This SHG is used as a criterion to compare the effect of NBTI on different flip-flops. A smaller SHG is more desirable for designers since this would imply that the mean time to failure (NBTI-affected lifetime) of the circuits will be longer.

4. NBTI-AWARE FLIP-FLOP DESIGN

The variation in CSHT contour due to NBTI can cause a timing failure in the circuit. To overcome this failure the flip-flop must be designed in a way so as not to violate the timing constraints after aging effect. We present a technique for designing flip-flops to alleviate this problem.

In this section, we explore three different sizing techniques for alleviating the NBTI effect. The first two are the straightforward scenarios which have been proposed in the literatures to alleviate the NBTI effect in combinational circuits [5]. The last one is our proposed sizing technique.

a) Cell level sizing

One approach is to uniformly up-size all the transistors in the flip-flop to overcome the NBTI effect. The overhead of this approach is the area penalty and added power consumption. More importantly, as we will show later, this technique is inferior in NBTI alleviation. In Section 4.1 and 5, we show the result of this scenario for conventional master-slave FF and True single-phase clock FF (TSPC).

b) Uniform PMOS transistor sizing

Upsizing PMOS transistors may solve the NBTI effect on the rising transitions of the pull-up networks but it degrades the falling transition of the pull-down networks severely by increasing the load (diffusion capacitance in the output node and the input capacitance of the following gates). It also increases the area and the power consumption of the flip-flop.

c) Selective transistor-level sizing (STLS)

We propose a selective transistor-level sizing approach for each flip-flop. We analyze each flip-flop circuit separately and modify the size of the NMOS and PMOS transistors in the circuit to compensate for the NBTI-induced shift of the CSHT contour. We also consider minimizing the area and power consumption of the circuit. More precisely, NBTI effect causes increase in the t_{c2q} as well as a right upward shift of the CSHT contour. To compensate for this aging effect, we will first judiciously size transistors in the flip-flop circuit in order to reduce its fresh (NBTI-unaffected) t_{c2q} so that the aged (i.e., at the end of the circuit lifetime) t_{c2q} of the new design is the same as the fresh t_{c2q} of the original design. Next, we intersect the 3-D clock-to-q surface of the new design with the fresh t_{c2q} of the original design to obtain an initial CSHT contour. From Figure 3 (c) this (new) contour will lie below and to the left of the (original) CSHT contour which is obtained by intersecting the 3-D clock-to-q surface of the original design with the fresh t_{c2q} of the original design. Therefore, after aging the new CSHT contour will gradually move and approach the original CSHT contour due to NBTI effect (see Figure 7).

Details of the sizing approach are described next.

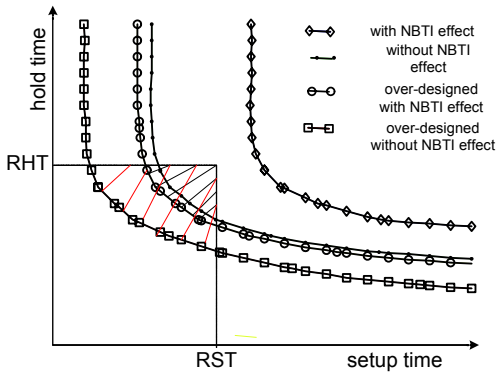

Figure 7. Flip-flop design.

4.1 Conventional Master-Slave Flip-Flop

In this section, we apply our *selective transistor-level sizing* (*STLS*) technique on a master-slave flip-flop (MSFF) which comprises transmission gates (TGs) and inverters as depicted in Figure 8.

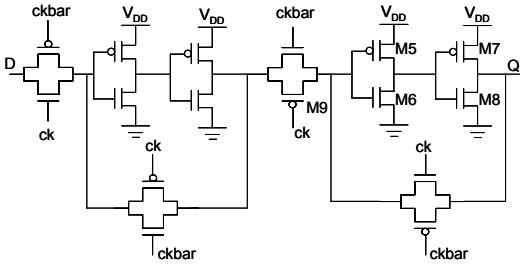

Figure 8. Negative-edge triggered master-slave flip-flop.

Recall that the NBTI effect degrades the low-to-high propagation delay and rise time at the output of CMOS inverters. Sizing up all transistors in these inverters is not the answer since sizing up one inverter will speed up that inverter but will also slow down the preceding inverter due to increased loading. Similarly, sizing up only the PMOS transistors in the four inverters is not effective since it will improve the speed of one inverter (which is making a

low-to-high transition) only to degrade the switching speed of the other series connected inverter in the loop (which is obviously making a high-to-low transition); hence the overall performance of the sized MSFF remains relatively unaffected. There is also the issue of increased loading everywhere due to sized-up PMOS transistors. Hence, we use STLS technique to selectively size different transistors to overcome the NBTI effect. To do so, we observe that the setup time of this flip-flop is dependent on the delay of the left TG and to some extent the delay of the series inverters in the master latch. The hold time is negative while the clock-to-q delay is a function of the delay of the right TG and delays of the two series inverters in the slave latch (see Figure 8). Following the design approach described above, we end up with the size of M5, M6, M7, M8, and M9 being increased by 36%, 25%, 30%, 20%, and 15%, respectively. Note that this sizing solution decreases the fresh clock-to-q delay of the new flip-flop design. The area and power consumption of the MSFF are increased by 8.3% and 7.64%, respectively. Starting with this new design, we simulate the circuit to capture the NBTI effect after three years of flip-flop usage. The result is an aged CSHT contour with SHG=0.31.

The effects of the three design approaches, i.e., cell level sizing, uniform PMOS transistor sizing, and STLS, on MSFF are shown in Figure 9 and Table 1. From Figure 9 one can see that cell level sizing and uniform PMOS transistor sizing indeed are not effective to suppress the NBTI effect on MSFF, whereas STLS is very efficient.

Table 1: Over-design techniques comparison for MSFF

Sizing Technique	SHG	area increase	power consumption increase
cell level sizing	0.41	+26%	+19.8%
uniform PMOS transistor-level sizing	0.71	+14%	+11.52%
selective transistor-level sizing	0.31	+8.3%	+7.64%

5. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, we validate our claims about the change in setup/hold time codependency of flip-flops due to NBTI effect and show that our over-design technique is very effective. We also compare MSFF and True Single-Phase Clock (TSPC) to see in the presence of NBTI effect, which one is more robust.

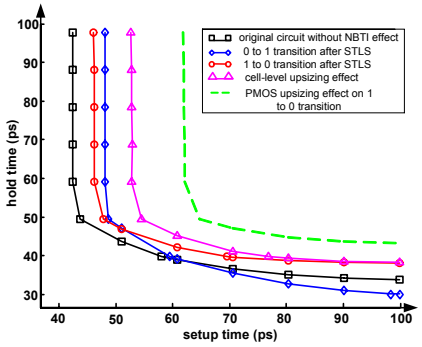

Figure 9. Master-slave flip-flop design verification.

5.1 True Single-Phase Clock Flip-Flop

The positive edge TSPC flip-flop is shown in Figure 10 features positive setup and hold times. As a result of three years of aging due to the NBTI effect and assuming a data input probability of 0.5, as reported in Figure 11, Δx_{SLB}=9ps and Δy_{HLB}=3.6ps. So, SHG=0.24.

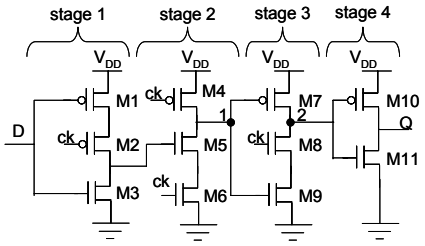

Figure 10. Positive edge-triggered flip-flop in TSPC.

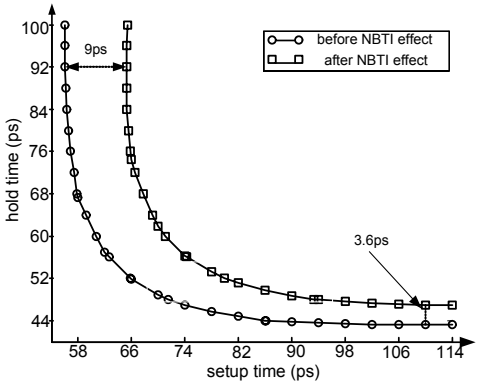

Figure 11. TSPC flip-flop NBTI tolerance measurement.

The tolerance measurement of the MSFF is also shown in Figure 12. As one can see from this figure, the shift of the contour for MSFF (Δx_{SLB}=24ps and Δy_{HLB}=10ps. So, SHG=0.88) is much larger than that of TSPC. The reason for the lower impact of NBTI on TSPC is the topology of its circuit. All the PMOS transistors in the circuit have inputs with duty cycle of 50%. This means the PMOS transistor is in the recovery mode half of the time (is assumed that the duty cycle of clock is 50%). In addition, in half of the clock cycle, transistor M4 is pre-charged to V_{DD} and this sets the gate voltage of transistor M7 to V_{DD} for half of the circuit's lifetime. Assuming the probability of the data input is 0.5, in 75% of the circuit lifetime, the gate voltage of M7 is at V_{DD}, which means that M7 is in the recovery mode.

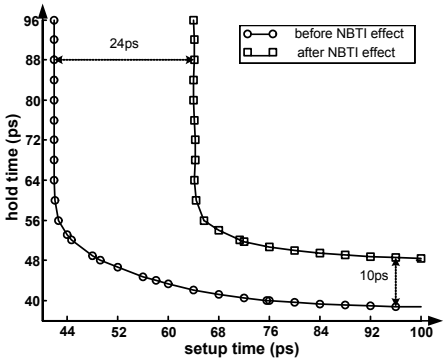

Figure 12. Master-slave flip-flop NBTI tolerance measurement.

5.2 TSPC Flip-Flop Selective Transistor-Level Sizing

In this section, we apply our selective transistor-level sizing approach to minimize the NBTI effect on the TSPC FF. The setup time is equal to the delay of the stage 1 (clocked) inverter whereas the clock-to-q delay is related to the summation of delays of the last three stages of the flip-flop. The hold time is the difference of the falling delays of stage 1 and stage 2 inverters. To decrease t_{c2q}, we modify the size of transistors in stages 2 to 4. It should be noticed that as a result of NBTI effect, the output transition from 0 to 1 becomes slower. When the clock becomes high and the input has a transition from 0 to 1, the pull-down network of the third stage of the FF must be fast enough to make the output transition from 0 to 1 faster. Since in TSPC, during the pre-charge phase, node 1 is always connected to V_{DD} through M4, transistor M9 is already ON. Therefore, one only needs to make transistor M8 faster by increasing its size. On the other hand, the output transition from 1 to 0 should not be allowed to degrade. The selective sizing through STLS is thus achieved by increasing the size of M8, M10 and M11, each by 20%.

Figure 13 shows the effect of cell level sizing, uniform PMOS sizing, and STLS on TSPC flip-flop. From this figure one can see that in the case of STLS, SHG=0.007. Furthermore, it can be seen that unlike MSFF, cell-level sizing is effective in suppressing NBTI effect; however, as shown in Table 2, the area and the power consumption overhead of cell-level sizing is significant, whereas the power and area overhead of STLS technique is negligible. Finally, by comparing Table 1 and Table 2 one can conclude that TSPC flip-flop is more robust than MSFF. This is mainly due to the topology of the circuits and the amount of time that PMOS transistors spend in the recovery mode.

Table 2: Over-design techniques comparison for TSPC

Sizing Technique	SHG	Area increase	power consumption increase
cell level sizing	0	+40%	+24.1%
uniform PMOS transistor-level sizing	0.50	+20%	+9.67%
selective transistor-level sizing	0.007	+6%	+0.85%

6. CONCLUSION

In this paper, we studied the NBTI effect on the setup/hold time codependency of flip-flops. We showed different flip-flop types have different vulnerability to NBTI effect and defined a criterion to quantify this liability. We showed that in general, uniformly sizing all PMOS transistors of a flip-flop is not that effective in reducing the NBTI effect. Consequently, we showed how to size the transistors of master-slave and true single phase clock flip-flops to minimize the effect of NBTI on criticality (tightness) of timing constraints which are imposed on the flip-flops. Experimental results proved the efficacy of the proposed sizing technique.

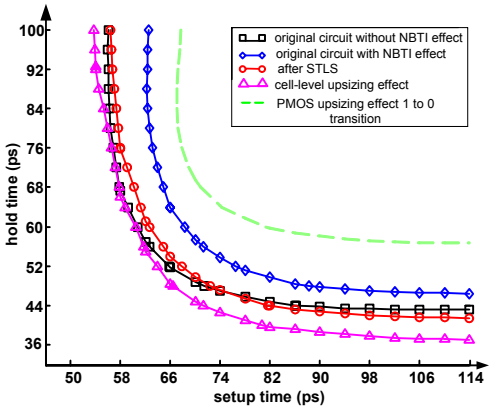

Figure 13. TSPC flip-flop design verification.

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