Low-power Sequential Circuit Design Using T Flip-flops

XUNWEI WU**†** and MASSOUD PEDRAM**††**

Abstract

This paper presents a novel circuit design technique to reduce the power dissipation in sequential circuits by using T flip-flops. The unwanted triggering action of the master clock to flip-flops can be isolated during T = 0. An example design of a decimal counter demonstrates the large power saving and improved performance of the resulting circuit.

1. Introduction

In the past, the major concerns of the VLSI designer were area, performance, and cost; power consumption considerations were mostly of secondary concern. In recent years, however, this trend has begun to change, and, increasingly, power consumption is being given comparable weight to area and speed in VLSI design (Rabaey and Pedram 1996). One reason is that the continuing increase in chip scale integration and the operating frequency has made power consumption a major design issue in VLSI circuits. The excessive power dissipation in integrated circuits not only discourages their use in a portable device, but also causes overheating, which degrades performance and reduces the circuit lifetime. All of these factors drive designers to devote significant resources to reduce the circuit power dissipation. Indeed, the Semiconductor Industry Association identified low-power design as a critical technological direction in 1992.

In CMOS circuits, the dominant component of power dissipation is that which is required to charge or discharge the capacitors in the circuit. The power dissipation of a node in the circuit is expressed by the following equation:

$$P = 0.5 C_L \cdot V_{DD}^2 \cdot f_{CLK} \cdot E_{SW}$$

where C_L is the physical capacitance at the node, V_{DD} is the supply voltage, f_{CLK} is the clock frequency, E_{SW} (referred to as the average switching activity) is the average number of output transitions per clock cycle $1/f_{CLK}$.

The sequential circuit elements in a CMOS circuit are considered major contributors to the power dissipation since one of the inputs of sequential circuit elements is the clock, which is the only signal that switches all the time. In addition, the clock signal tends to be highly loaded. To distribute the clock and control the clock skew, one must construct a clock network (often a clock tree) with clock buffers. All of this adds to the total node capacitance of the clock net, which also happens to have the largest activity (two transitions per cycles) in a synchronous circuit (ignoring possible hazard activity on the same signal lines). Recent studies indicate that the clock signals in digital computers consume a large percentage (15% - 45%) of the system power. Thus, reducing the clock power dissipation can greatly reduce the power dissipation in digital VLSI circuits.

† Department of Electronic Engineering, Zhejiang University, Hangzhou, China.

†† Department of Electrical Engineering-Systems, University of Southern California, Los Angeles, USA.

Most efforts for clock power reduction have focused on issues such as voltage swing reduction, buffer insertion, and clock routing (Friedman 1994). In many cases clock switching causes a lot of unnecessary gate activity. For that reason, reducing or suppressing unwanted clock switching becomes an important way to reduce the power dissipation of sequential circuits. This goal can be achieved by two means.

The first method is to eliminate the wasted power dissipation caused by the clock's switching in the non-triggering direction. The flip-flops now available are all Single-Edge Triggered (SET), that is, they are only sensitive to the clock's falling edges. Therefore, power dissipation caused by the clock's rising edge is wasteful. For this reason, Double-Edge Triggered (DET) flip-flops have been developed which switch at both the falling and the rising edges of the clock (Unger 1981, Lu and Ercegovac 1990, Afghahi and Yuan 1991, Gago *et al.* 1993, Hossain *et al.* 1994, Pedram *et al.* 1997,). Consequently, the clock frequency can be reduced by half while keeping the same data rate, resulting in 50% power savings in the flip-flops.

The second method is to block the clock signal feeding into the flip-flops during their holding states so as to reduce the power dissipation. In this case the clock received by the flip-flop should not be the chip master clock. This means that other clocks must be derived from the master clock that can be slowed down or stopped completely with respect to the master clock under certain conditions. Obviously, this scheme results in power savings due to the following factors:

i) Load on the master clock as well as the number of required buffers in the clock tree is decreased. Therefore, the power dissipation of the clock tree is reduced.

ii) The flip-flop receiving the derived clock is not triggered in idle cycles; hence, the corresponding dynamic power dissipation is saved.

iii) The excitation function of the flip-flop triggered by a derived clock may be simplified since it has a don't-care condition in the cycle when the flip-flop is not triggered by the derived clock.

According to the above analysis several techniques were presented for saving power in the clock tree by stopping the clock fed into idle modules (Tellez 1995, Benini *et al.* 1994, Benini and De Micheli 1996). However, a number of engineering issues related to the design of the clock tree were not addressed.

On the other hand, in conventional design we are interested in the next state of a flip-flop; hence, D flip-flops are the natural choice for CMOS circuits. In low power design, we are more concerned with whether or not the next state changes; hence, T flip-flops become the preferred choice. Notice that the switching of the output of a T flip-flop is controlled by the excitation input T. The clock power dissipation occurs during both T=0 and T=1. However, it is desirable to eliminate the clock power dissipation during T=0. This can be accomplished by using the excitation function for input T to control the clock. This idea is very effective in reducing the clock power, and, as we will show during the design of a decimal counter, the use of T flip-flops (instead of D flip-flops) leads to simpler combinational logic and, hence, further power reduction.

Based on the above discussion, this paper describes how to generate a secondary clock that is derived from the clock tree, is glitch-free, and has no additional skew. Next, we introduce the don't-trigger signal and show how to use T flip-flops for designing sequential

2

circuits, which have lower dissipation and simpler combinational logic. Circuit simulation is used to check the quality of the derived clock and its ability to reduce the power dissipation of the sequential circuits.

2. Gating the clock by using a don't-trigger signal

If there are flip-flops whose inputs are unchanged when a sequential circuit goes from one state to the next, we can produce a *don't-trigger signal* $\overline{T}$ from the original state to cutoff the path from the master clock to these flip-flops. As a result, these flip-flops are not subjected to the clock signal and their power dissipation is reduced accordingly.

Without loss of generality, consider that the flip-flops in the sequential circuit are sensitive to the clock's falling edge. Fig.1(a) shows that $\overline{T}$ is directly used to control the OR gate to cutoff the master clock clk; the derived clock is $clk' = \overline{T} + clk$. Fig.1(d) shows the timing relationship of $\overline{T}$, clk, and clk'. This scheme fails, however, because of the following reasons:

i)   Suppose that $\overline{T}$ is produced in cycle S_1 and disappears in cycle S_3, that is, the output of the flip-flop should remain unchanged during the $S_1 \rightarrow S_2$ and $S_2 \rightarrow S_3$ transitions. However, the waveform of clk' in Fig.1(d) shows that the falling transition of $\overline{T}$ in cycle S_3 causes an unwanted transition that should have been avoided since $\overline{T} = 1$ when $S_2 \rightarrow S_3$.

ii) The derived clock clk' has a long delay of $t_f + t_d + t_g$ with respect to the master clock, where t_f is the delay time of flip-flop, t_d is the delay time of the combinational circuit for generating the signal $\overline{T}$, and t_g is the delay time of the OR gate in Fig.1(a).
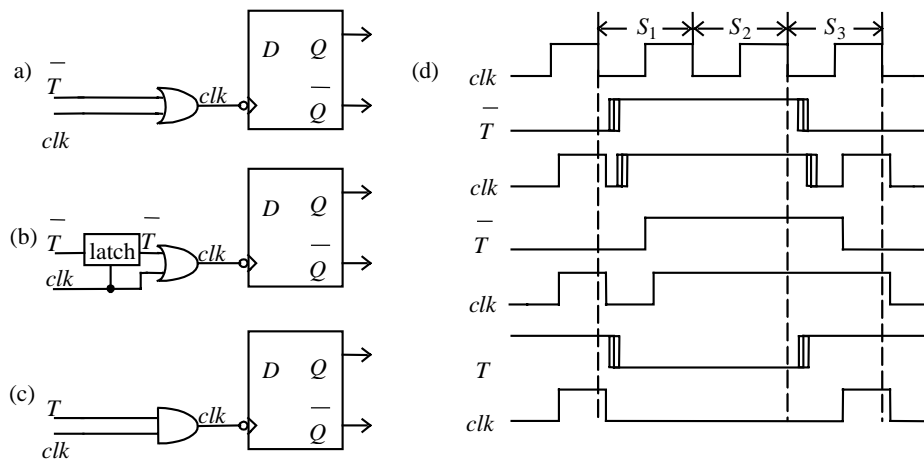

Figure 1. Don't-trigger signal controls the master clock

(a) Cutoff the master clock through an OR gate,

3

iii) If the combinational circuit for generating $\overline{T}$ has race hazards which appear after the master clock falls ($clk = 0$), these hazards may propagate to the derived clock clk' through the OR gate in Fig.1(a).

In Ref.[6], the authors propose a scheme whereby a latch is used to filter out hazards and synchronize $\overline{T}$ with the master clock as shown in Fig1(b). Because the latch is in the storage state during $clk = 0$, the incidental glitch of $\overline{T}$ can be filtered out, and the derived $\overline{T}'$ is able to cutoff the master clock during state transitions $S_1 \rightarrow S_2$ and $S_2 \rightarrow S_3$. The derived clock clk'' is obtained as shown in Fig.1(d). However, this scheme has the following shortcomings:

i) The added latch increases the circuit complexity.

ii) Since the master clock clk is connected to the newly added latch, the extra power dissipation of clk offsets some of the power saving due to the non-triggering of the flip-flop.

iii) There is still the t_g delay between the derived clock clk'' and the master clock clk, which results in the clock skew. As a result, the sequential circuit is not safely synchronized.
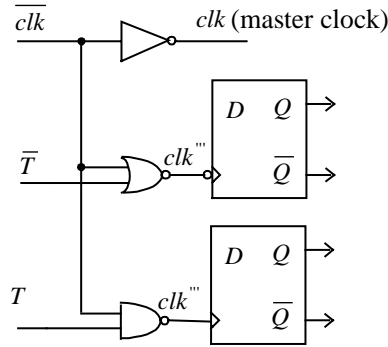

Figure 2. Quasi-synchronous clocks derived from the master clock

In fact, we can cut off the transmission of the clock by using the *trigger signal* T to control an AND gate, as shown in Fig.1(c). The derived clock clk''' is shown in Fig.1(d). It will not carry glitches since $clk = 0$ blocks possible glitches on signal T by the AND gate. Besides, this scheme has an obvious advantage due to the omission of the appended latch, but it does not solve the clock skew problem. A simple idea is to appropriately delay the clk and then use it as the master clock. In this way the delayed master clock will be synchronous with respect to clk''', which means that the clock skew between clk''' and clk can be made very small by the appropriate sizing of transistors in the NOR gates. This leads to another idea in which the presence of both clk and $\overline{clk}$ in the clock tree can be exploited. In particular, if we rewrite $clk''' = T \cdot clk$ as $clk''' = \overline{\overline{T} + \overline{clk}}$, where $\overline{clk}$ is taken from the previous stage of the clock

4

tree, then we can design a synchronous derived clock based on the NOR gate, as shown in Fig.2. As long as we control the delay of the inverter to make it nearly the same as that of the NOR gate in Fig.2, the skew between clk and clk''' will be very small; thus the derived clock clk''' will be synchronous with respect to clk. We should note that in the above discussion the transition of signal $\overline{T}$ occurs during $\overline{clk} = 1$. Consequently, the transition itself and any possible glitch on $\overline{T}$ are blocked. However, if the delay time for generating $\overline{T}$ is too long, then it becomes possible for the transition or for the glitches to appear during $clk = 1$.

In Fig.2, we also offer the circuit to produce the synchronous derived clock based on a NAND gate that is controlled by T. This design is suitable for flip-flops that trigger on the rising clock edge. This clock-gating scheme is directly derived from Fig.1(c) and is hazard-free subject to the abovementioned condition for the negative-edge triggered flip-flops. Notice that the two flip-flops in Fig.2 can be considered T flip-flop if their excitation inputs D are connected with their outputs $\overline{Q}$.

3. Design of sequential circuits using T flip-flops

The D flip-flop is widely used in the design of CMOS sequential circuits. However, when the don't-trigger signal $\overline{T}$ is used to gate the master clock's triggering action to the flip-flops, the T flip-flop function is a better choice. The next-state equation of a T flip-flop is $Q_+ = T \oplus Q$, therefore we set $T = Q \oplus Q_+$ which indicates that the flip-flop switches or holds state during $T = 1$ or $T = 0$, respectively. This equation matches with the method of using the don't-trigger signal $\overline{T}$ to gate the master clock as mentioned in previous section. So we only need to use the T function from the T flip-flop design to gate the master clock.

Taking a decimal counter as an example, the next state of the counter is shown in Table 1. If D flip-flops are used as is typically the case, we will obtain Karnaugh maps for the excitation functions D_3, D_2, D_1, and D_0 from the next states in Table 1, as shown in Fig.3(a). In these maps, an empty box represents the don't-care condition. The optimized excitation functions are:

Table 1. State table of a decimal counter

Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1

| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

$$D_3 = Q_2 Q_1 Q_0 + Q_3 \overline{Q_0},$$

$$D_2 = Q_2 \oplus (Q_1 Q_0),$$

$$D_1 = \overline{Q_3}\,\overline{Q_1} Q_0 + Q_1 \overline{Q_0},$$

$$D_0 = \overline{Q_0}.$$

The corresponding circuit realization is shown in Fig.3(b) which is a traditional synchronous design for a decimal counter.
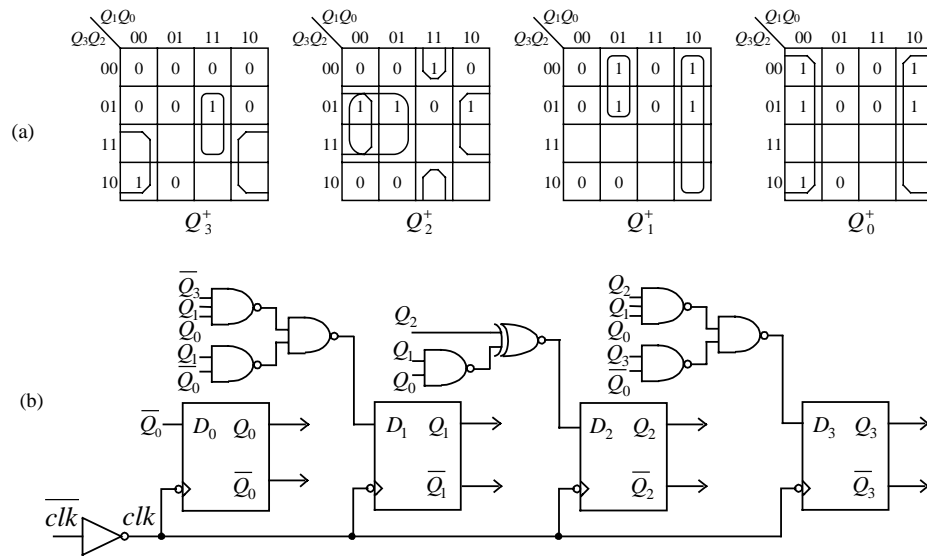

Figure 3. Synchronous design of a decimal counter

(a) Karnaugh maps of D_3, D_2, D_1, and D_0, (b) circuit realization

Now we use T flip-flops in the design instead of D flip-flops. Since $T = Q \oplus Q_+$, as shown in the next-state Karnaugh maps in Fig.3(a), the Karnaugh maps of the excitation functions T_3, T_2, T_1, and T_0 are obtained as shown in Fig.4(a). The optimized excitation functions are:

$$T_3 = Q_3 Q_0 + Q_2 Q_1 Q_0 = (Q_3 + Q_2 Q_1)Q_0,$$

$$T_2 = Q_1 Q_0,$$

$$T_1 = \overline{Q_3} Q_0,$$

$$T_0 = 1.$$

Assuming that the D flip-flops are sensitive to the falling edge of the clock signal, we can adopt the method of producing a derived clock based on the NOR gate in Fig.2. The clock signals for these four flip-flops are:

$$clk_3 = T_3 \cdot clk = \overline{\overline{T_3} + \overline{clk}} = \overline{\overline{Q_3 + Q_2 Q_1} + \overline{Q_0} + \overline{clk}},$$

$$clk_2 = T_2 \cdot clk = \overline{\overline{T_2} + \overline{clk}} = \overline{\overline{\overline{Q_1} + \overline{Q_0}} + \overline{clk}},$$

$$clk_1 = T_1 \cdot clk = \overline{\overline{T_1} + \overline{clk}} = \overline{\overline{Q_3 + \overline{Q_0}} + \overline{clk}},$$

$$clk_0 = T_0 \cdot clk = \overline{\overline{T_0} + \overline{clk}} = \overline{\overline{\overline{clk}}}.$$

From the clock functions, we construct the circuit realizations shown in Fig.4(b). Notice that in this circuit, to derive clk_3, the n part of the CMOS configuration for realizing $\overline{Q_3 + Q_2 Q_1}$ is composed of two series nMOS transistors parallel-connected with an nMOS transistor, and the p part is composed of three pMOS transistors with dual configuration (Weste and Eshraghian 1993). So the complexity of the circuit for realizing $\overline{Q_3 + Q_2 Q_1}$ is equal to that of a 3-input NOR gate. From this, the circuit construction in Fig.4(a) is clearly simper than its counterpart in Fig.3(a).
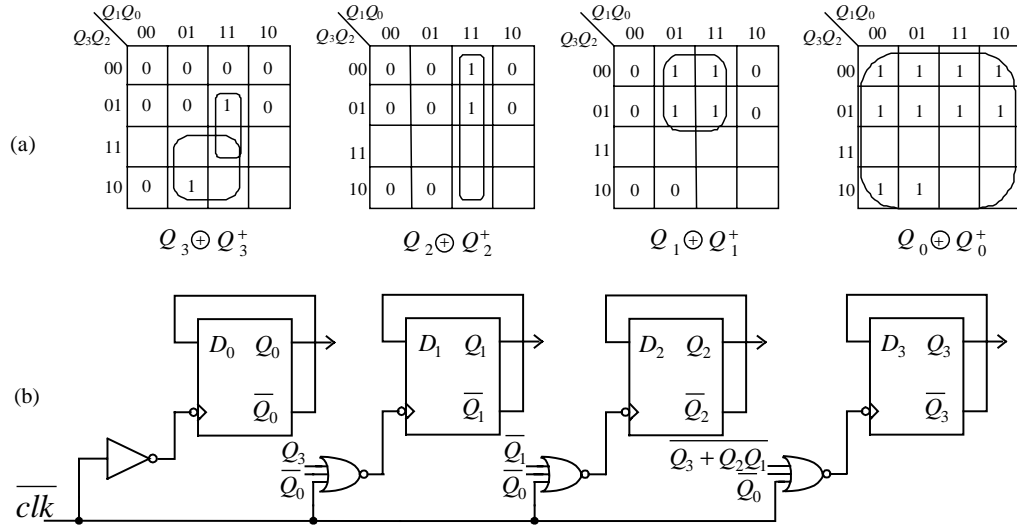

Figure 4. Quasi-synchronous design of a decimal counter

(a) Karnaugh maps of T_3, T_2, T_1, and T_0, (b) The circuit realization

The simple construction of the combinational circuit results in lower power dissipation. However the low power dissipation property is mostly achieved as a result of gating the clock. Besides flip-flop Q_0, the three flip-flops Q_3, Q_2, and Q_1 have no dynamic power dissipation when there is no clock triggering.

We simulated the new design in Fig.4(b) by PSPICE with 0.5μ CMOS technology. The transient analysis shown in Fig.5 proves that the new design has the expected logic operation.

7

The Q-to-$\overline{clk}$ average delays for the four flip-flops are listed in Table 2, which shows that the flip-flops in Fig.4(b) can be switched synchronously. For comparison, the delays of the synchronous design in Fig.3(b) are also given in the table. As we can see, the average delays are comparable.

Table 2. Average delay of flip-flops

	Q_0	Q_1	Q_2	Q_3
Design in Fig.4(b)	0.252ns	0.259ns	0.261ns	0.276ns
Design in Fig.3(b)	0.463ns	0.453ns	0.403ns	0.402ns

We also measure the power dissipation of the synchronous design in Fig.3(b) and the quasi-synchronous design in Fig.4(b). The energy dissipation diagrams are shown in Fig.6 and prove that the later design reduces the power dissipation by 51%. This is expected since the clk_1, clk_2, and clk_3 waveforms in Fig.5 show that in a decimal counting cycle, flip-flops Q_1, Q_2, and Q_3 are triggered only 4, 4 and 2 times, respectively. Furthermore, we know that they have no dynamic power dissipation when not triggered and that the simpler combinational circuit in Fig.4(b) has a simpler structure which results in low power dissipation.
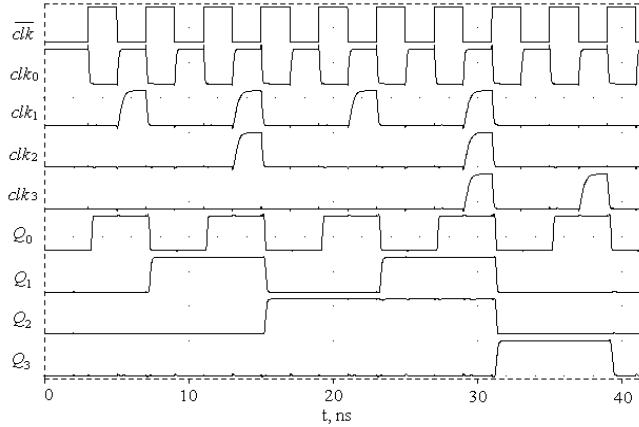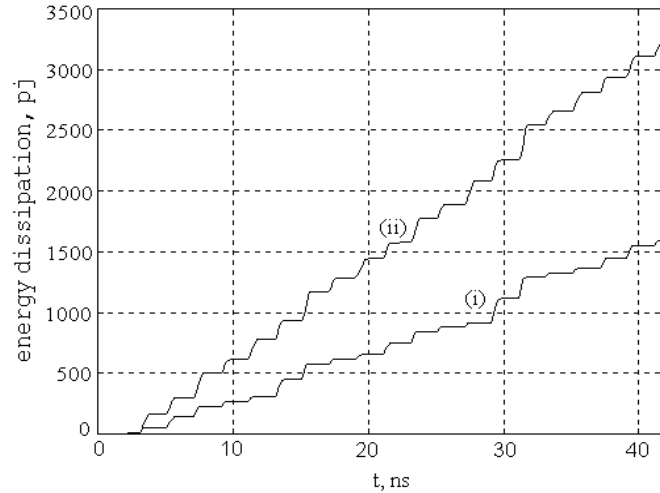

Figure 5. Transient analysis

Figure 6. Energy dissipation versus time

(i) Quasi-synchronous design of a decimal counter

(ii) Synchronous design of a decimal counter

4. Conclusions

We presented a procedure for gating the clock by means of the don't-trigger signal. The derived clock is synchronous with respect to the master clock and can be used to isolate the triggered flip-flops from the master clock in their idle cycles. The achieved power saving is significant as shown by the example design of a decimal counter. The circuit simulation proved the quality of the new derived clock and its ability to reduce power dissipation. Thus, the engineering issues related to the use of gated clocks have been resolved for practical applications, opening the path for adoption of the clock-gating technique in the design of low-power sequential circuits.

This paper presented a new design style for sequential circuits. In traditional design engineers are concerned with the next state of a flip-flop. Thus the D flip-flop, whose next state is controlled by the excitation input D, is the natural choice. In low-power design, instead, we are concerned with whether or not a flip-flop switches its state. If the flip-flop remains in its original state the corresponding dynamic power dissipation can be avoided. Thus, the T flip-flop, whose switching is controlled by the excitation input T, becomes a reasonable choice. However, in a traditional T flip-flop, the power dissipation caused by the clock still cannot be avoided during T=0.

In this paper we used the T function to control the clock instead of the excitation input, thereby we achieved power saving during T=0. It should be pointed out that the proposed circuits tend to incur additional area overhead compared to a conventional sequential logic design that uses T flip-flops. However, if we compare the proposed circuits with a conventional sequential logic design that uses D flip-flops, the proposed circuits tend to result in simpler combinational logic in terms of the gate count or silicon area. The design of a decimal counter in this paper demonstrated this area savings. In fact, the new design style using T flip-flops

9

offers an important, new design choice for sequential circuits.

Acknowledgments

References

AFGHAHI, M. and YUAN, J., 1991, "Double edge-triggered D-flip-flops for high-speed circuits," *IEEE J. Solid-State Circuits*, **26**, 1168-1170.

BENINI, L., SIEGEL, P. and DE MICHELI, G., 1994, "Saving power by synthesizing gated clocks for sequential circuits," *IEEE Design & Test of Computers*, Winter, 32-41.

BENINI, L. and DE MICHELI, G., 1995, "Transformation and synthesis of FSMs for low power gated clock implementation," *Proc. Int. Symp. Workshop on Low Power Design*, Dana Point, 21-26.

FRIEDMAN, G., 1994, Clock distribution design in VLSI circuits: an overview, *Proc. IEEE Int. Symp. On Circuits and Systems*, San Jose, 1475-1478.

GAGO, A., ESCANO, R. and HIDALGO, J. A., 1993, "Reduced implementation of D-type DET flip-flops," *IEEE J. Solid-State Circuits*, **28**, 400-402.

HOSSAIN, R., WRONSKI, L. D. and ALBICKI, A., 1994, "Low power design using double edge triggered flip-flops," *IEEE Trans. VLSI Systems*, **2**, 261-265.

LU, S. L. and ERCEGOVAC, M., 1990, "A novel CMOS implementation of double-edge-triggered flip-flops," *IEEE J. Solid-State Circuits*, **25**, 1008-1010.

PEDRAM, M., WU, Q. and WU, X., 1998, "A new design of double edge triggered flip-flops," *Proc. Asia-Pacific Design Automation Conf.*, Yokohama, 417-421.

RABAEY, J., and PEDRAM, M., 1996, *Low Power Design Methodologies*, Kluwer Academic Publishers.

TELLEZ, G. E., FARRAH, A. and SARRAFZADEH, M., 1995, "Activity-driven clock design for low power circuits," in *Proc. IEEE Int. Conf. on Computer Aided Design*, San Jose, 62-65.

UNGER, S. H., 1981, "Double-edge-triggered flip-flops," *IEEE Trans. Computers*, **30**, 447-451.

WESTE, N. H. E. and ESHRAGHIAN, K., 1993, *Principles of CMOS VLSI Design: A System Perspective*, 2nd Edition, (New Work: Addison-Wesley Publishing Co.).