Multi-code state assignment for low power design

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Abstract: This paper proposes a multi-code state assignment to realize the priority encoding by restraining redundant states. It is indicated that a state assigned with multi-code can be allocated using fewer state variables; Furthermore flip-flips corresponding to the absent state variables can be clock-gated. An algorithm is presented to implement the multi-code state assignment for general sequential circuits. As a result, lower power dissipation may be attained. Practical design examples are simulated by PSPICE and demonstrate that this technique can lead to sizable power saving.

1 Introduction

The direct synthesis of sequential circuits for low power[1~5] is an area of exploration which promises more global power saving. The sequential circuit design can be divided into the following steps: (1) State reduction (for determining the number of state variables); (2) State assignment (for determining the corresponding relation between states and state variable values); (3) Choice of flip-flops (the number of flip-flips is equal to that of state variables); (4) Design of the combinational circuit part (for providing the outputs and next states). State assignment has an important role in determining the overall in terms of the number of nodes required to implement the output and next logic. On the other hand, state assignment directly affects the switching activity of the state variables and the interior variables in the circuit. We know that both the number of nodes and the switching activity influence the power dissipation of combinational circuit. From this, we realize that state assignment is the critical step in low power design of sequential circuit.

During the low-power design of combinational circuits we have found that blocking the redundant signals and shutting off the redundant parts in circuit is effective method to lower the energy dissipation. If a certain part of the circuit has no effect on the circuit functionality during some time period, it is called redundant. If this part stops working (by cutting off the power supply or by fixing its input signals), energy saving can be obtained. For the design of sequential circuits, this technique of exploiting redundancy can be executed in the low power dissipation corresponding combinational logic parts. Compared with a combinational circuit, however, there are several special design aspects in a sequential circuit:

(i) A sequential circuit has filp-flops, which store state signals.

(ii) A sequential circuit has special clock signals to synchronously trigger flip-flops so as to realize the synchronous switching of state variables

(iii) States are assigned by encoding state variables.

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We next describe three restraining techniques with respect to each of these aspects:

(i) Traditional flip-flops are single-edge triggered flip-flips (SETFF), which is sensitive to rising or falling edge of the clock. So half of the clock's transitions have nothing to do with the circuit and become redundant behaviors, which in turn results in wasteful dynamic energy dissipation in these flip-flops. For this reason, a double-edge triggered flip-flop (DETFF) can be used, which utilizes both transition edges of the clock, and thereby achieve energy saving. [6-8]

(ii) The function of the clock is to force all flip-flips to change their state synchronously (present state to next state). During this switching process, if a certain flip-flop's next state is the same as its present state, then this flip-flip is in a holding mode. The clock's triggering for it is redundant and can be masked. Therefore, a clock gating technique was developed to lower the energy dissipation, and it works. [9-11]

(iii) In the state assignment, *k* state variables are used to express 2^k different states. However, if the number of working states l is not equal to 2^k, $l \le 2^k$, there will exist $(2^k - l)$ redundant states in state assignment. Of course, these redundant states are beneficial in reducing the complexity of the combinational circuit, but the reliability of the circuit may be influenced. We have to consider the system's behavior if it enters into one of these redundant states and have to make the system self-corrective. Theoretically, there should be a technique for avoiding the redundant states, which is useful for saving power, but we have however not seen any work in this field up to now.

This paper proposes a multi-code state assignment to avoid encountering redundant states. The result of multi-code state assignment is that some states do not require binary assignment of all state variables. When the system is in such a state, the unused state variables become redundant. From this principle, we will study the corresponding redundancy restraining technique and consider its availability in low power design of sequential circuits.

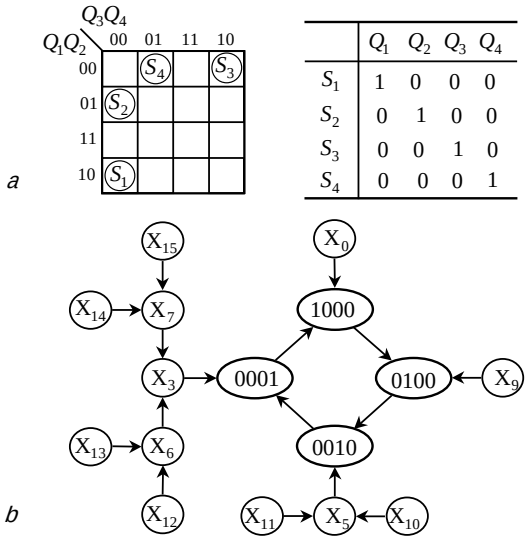
2 Priority encoding by using redundant states

In combinational circuit design, the existence of redundant states is helpful in generating a larger prime implicant during Boolean optimization. If the implicant contains 2^m minterms, a maximum of m variables may be reduced in the product-form. If we use k state variables to express l different states ($l \le 2^k$) thus there will be $(2^k - l)$ redundant states.

In fact, we may change the uni-code state assignment where a state code corresponds to a state variable minterm. The $(2^k - l)$ redundant states may be utilized to make some states multi-coded, such as two-code assigned, four-code assigned, etc. These corresponding state assignments are equal to the larger implicates in combinational circuit design, which have fewer state variables. Thus it can be seen that those absent variables are redundant when the system is in these states. Because the corresponding flip-flops outputs are not being used, these flip-flops can be isolated from the clock so as to reduce their dissipation.

A special example of sequential circuit with a lot of redundant state is the one-hot ring counter, where each state corresponds to a state variable. Take four-state (S_1, S_2, S_3, S_4) counter as example, Fig. 1*a* shows the state assignment Karnaugh map and the state assignment table of the four states corresponding to four state variables (S_1, S_2, S_3, S_4). Notice that each state is encoded

by a state variable minterm, the result is twelve $(12 = 2^4 - 4)$ redundant states, which are expressed by blank cells in Fig. 1*a*. Although these redundant states can be used to simplify the exciting functions ($D_1 = Q_4$, $D_2 = Q_1$, $D_3 = Q_2$, $D_4 = Q_3$), the problem is that the design is not self-corrective. So we change D_1 as $D_1 = \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3$, to meet this requirement. The complete state diagram of the revised circuit is shown in Fig. 1b. We can see that if the circuit falls into one of the invalid states, it will return to the valid working cycle in a period no more than three clock cycles.



	Q_1	Q_2	Q_3	Q_4
S_1	1	0	0	0
S_2	0	1	0	0
S_3	0	0	1	0
S_4	0	0	0	1

Fig.1 *One-hot ring counter*

a K-map and tabular of state assignment

b Complete state diagram of revised self-corrective design

Now we use these twelve redundant states to realize the multi-code state assignment, as shown in Fig. 2*a*. In the state assignment table, state variable Q_4 is immaterial in any state, so it can be omitted and the four states can be re-encoded by three state variables. Because state S_4 is encoded by three zero state variables, this counter has evolved from a one-hot type to a one-zero-hot type.[12]

Because $Q^{'} = D$, the next state equation of the flip-flop, the exciting functions of the three flip-flops can be derived based on the state table shown in Fig. 2*b*:

$$D_1 = \overline{Q_1 + Q_2 + Q_3}\ ,\ D_2 = Q_1\ ,\ D_3 = Q_2$$

In Fig.2*b* S_1 is quad-coded and S_2 is double-coded in assignment while S_3 and S_4 are uni-coded. We found that Q_1 has the highest priority which means that if Q_1 =1, the values of other Q_2 , Q_3 are trivial. Besides, Q_2 has the second high priority in three state variables. Therefore, in the corresponding circuits, $Q_1 = 1$ can be used to restrain the switching of Q_2 and Q_3 , and $Q_2 = 1$ can be used to restrain the switching of Q_3 . This restraint function can be realized by a clock-gating technique, as shown in Fig.2c. We notice that the signal for gating the clock to Q_2 is D_1 rather than

Q_1. Reason is that when the clock comes, $D_1 = 1$ will make $Q_1 = 1$ and hence block the clock to Q_2 (and to Q_3) simultaneously. If delays of the two NOR gates, which produce the gated clock signals clk_2 and clk_3, are the same as that of the inverter which produces clk_1, then the three flip-flops work synchronously. Notice that the omitted fourth flip-flop is replaced by a NOR gate in the circuit.

The circuit of Fig.2*c* has been simulated by PSPICE. Fig. 3*a* shows waveforms of the three clock signals for the three flip-flops and the four outputs. Three clocks clk_1, clk_2, clk_3 are basically synchronous, and those four outputs Q_1, Q_2, Q_3, Q_4 prove that this circuit has correct logic functionality.

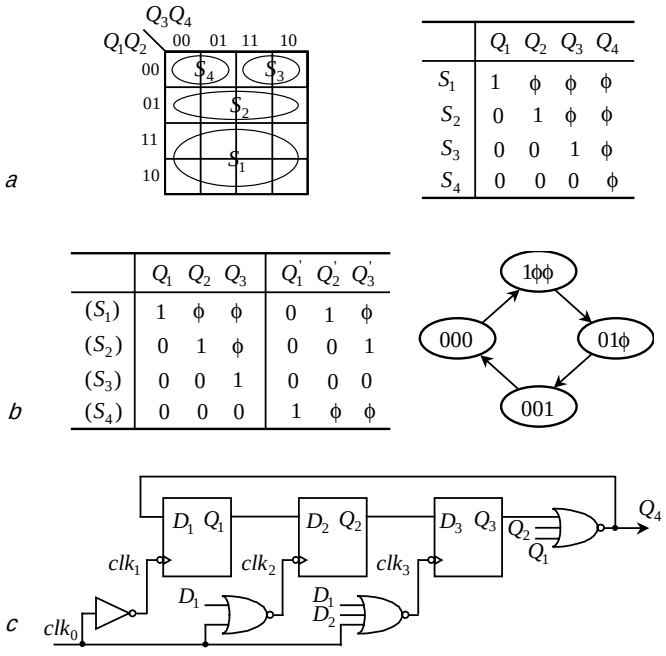


Fig. 2 *One-hot-zero ring counter*

a K-map and state assignment tabular

b State tabular and state diagram

c Design of clock gating

Now let's discuss the power dissipation in the new design. The state assignment table in Fig.1*a* shows that the four flip-flops receive 16 triggering actions from the clock in one cycle. However, the state assignment table in Fig.2*b* shows that the three flip-flops receive only 9 triggering actions from the clock in one cycle. Consequently, the power saving owing to reducing one flip-flop and gating clock should be $(16-9)/16 = 43\%$. The energy dissipation waveform of the two circuit in Fig.3*b* shows that the power saving is 33% in fact. The disparity is produced because of the energy dissipation in the NOR gates used for gating clock.

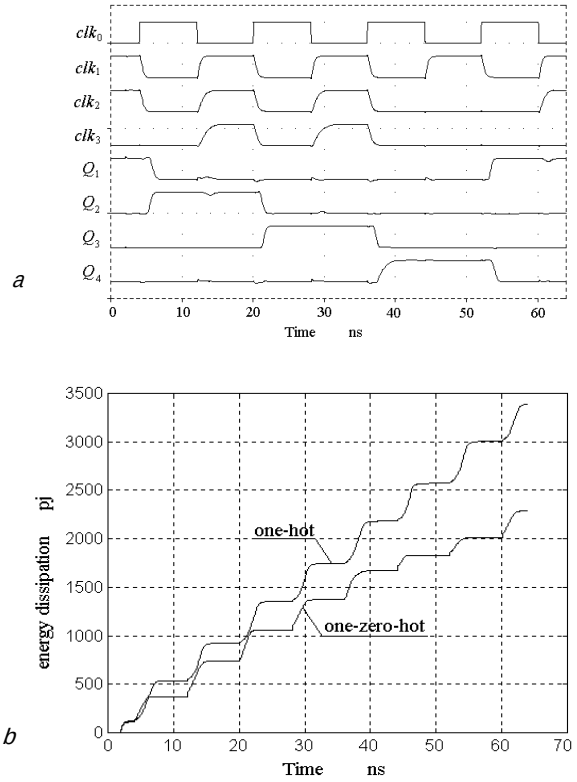


Fig. 3 *a* one-zero-hot counter's working waveform
b energy dissipation waveform

Finally, it should be pointed out that the design of Fig. 2*c* not only simplifies the circuit construction and saves the energy dissipation but also improves the circuit's reliability because of non-redundant state. The complete state diagram in Fig.2*b* shows this advantage.

3 Determination of multi-code state assignment

The uni-code state assignment corresponds to a minterm of the state variable space. In contrast, the multi-coded state assignment contains 2^m minterms of the state variable space. We have thus utilized or restrained $2^m - 1$ redundant states. Therefore, we can decompose the set of redundant states in groups of $2^i - 1$ states and determine the corresponding multi-code state assignment. In the last section, there were 12 redundant states when four state variables (Q_1, Q_2, Q_3, Q_4) are used, the non-redundant state assignment in Fig.2a is obtained according to 12 = 7+3+1+1. If we use three state variables (Q_1, Q_2, Q_3) instead, the number of redundant state is reduced to 4. Since 4 = 3+1, the non-redundant state assignment in Fig.2b is achieved. Evidently, the inclusion of redundant state in state assignment increases the complexity of the assignment procedure. We can modify however it on the basis of single-code assignment. This method both simplifies the procedure and maintains some characteristics of original design. We will take two sequential circuits in common use as examples to discuss the state assignment algorithm.

Example 1 Decimal up-counter

In this counter ten counting states (0, 1,…9) are encoded with the conventional 8421 BCD

encoding, as shown in the left of Table 1. Notice that there are 6 redundant states in this encoding: {1010, 1011, 1100, 1101, 1110, 1111}.

Table 1: Encoding of decade up-counter

	8421 BCD encoding				Priority-encoding			
digit	*D*	*C*	*B*	*A*	*D*	*C*	*B*	*A*
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	ϕ	ϕ	0
9	1	0	0	1	1	ϕ	ϕ	1

From the above table, the excitation functions for the four flip-flops can be derived as:

$$\begin{aligned} D_D &= CBA + D\overline{A}, \\ D_C &= C\overline{B} + C\overline{A} + \overline{C}BA, \\ D_B &= \overline{D}\,\overline{B}A + B\overline{A}, \\ D_A &= \overline{A}. \end{aligned} \tag{1}$$

Now we discuss the multi-code assignment by using six redundant states. Since 6 = 3+3, two states among ten digits can be quad-coded. Analyzing the original 8421BCD state encoding table, both states 9 and 10 can be quad-coded, as shown in the right of Table 1. This new scheme maintains the characteristics of original. As $D=1$ can be used to restrain state variables C and B, the priority of D is higher than C and B. In practical circuit, the output 1 of flip-flip D can be used to isolate the clock to trigger flip-flop C and flip-flop B so as to reduce the corresponding energy dissipation. It is not difficult to get the new excitation functions of four flip-flops:

$$\begin{aligned} D_D &= \overline{D}CBA + D\overline{A}, \\ D_C &= \overline{D}C + \overline{D}BA, \\ D_B &= \overline{D}\,\overline{B}A + B\overline{A}, \\ D_A &= \overline{A}. \end{aligned} \tag{2}$$

The comparison between eqn.1 and eqn.2 shows that D_B and D_A are the same in both sets. However, in the latter design, a literal $\overline{D}$ is added to D_D and the form of D_C is simplified. The result is that the combinational circuit part is simpler and the power dissipation is lower. As to the energy dissipation of flip-flops, the occurrence probability of each state in one cycle is 10%. From the right part of Table 1, as flip-flops C and B are restrained in states 8 and 9, they save 20% energy dissipation for themselves. As to all four flip-flops, the energy dissipation saving is 10%. Furthermore, the extra clock gating NOR gate leads to some additional energy dissipation.

In the above examples, the occurrence probability of each state was the same. In a general sequential circuit, however, each state's probability is not the same. To obtain the maximal power saving, a state with higher occurrence probability should be encoded first. The following algorithm

will produce a multi-code state assignment for the low power design based on the above example.

Algorithm 1 Given an initial state assignment scheme SA_0 for a sequential machine with a state set S and a redundant state set RS, the following steps will produce a multi-code state assignment with the low power dissipation.

1: If RS is empty, then return SA_0 and exit. Otherwise, let SA_{temp} be SA_0 and compute the occurrence probabilities of all the states in S based on the state table, then sort the states in descending order of probabilities.

2: For the first state s' with the highest probabilities in S, select a cube *c* as large as possible that covers s' and other redundant states, but not any other states in S. Hence s' is assigned with multi-codes covered by *c*. Then remove the redundant states covered by cube *c* from RS. Repeat this procedure for the next state until there is no remaining state in S or no redundant state left in RS.

3: Suppose the state assignment scheme obtained in step 2 is SA_1. Update SA_{temp} with SA_1 if its corresponding circuit needs less power dissipation. Then go to step 2 until there is no alternative selection of cubes for each state in S. This cube selection operation can be handled efficiently by the procedures proposed in ESPRESSO[13]. Update SA_{temp} each time when a better scheme is found.

4: If SA_{temp} and SA_0 are different, then replace SA_0 with SA_{temp} and go to step 1 with updated redundant state set RS; otherwise, go to step 5.

5: Return SA_{temp} as the final multi-code state assignment scheme.

Example 2 8421 BCD detector

An 8421 BCD detector receives a serial entry T, and four bits as a group (the less significant bit goes first). When it receives a group of non-8421 BCD entry, the output is $R=1$. The system's state table after reduction is shown in Table 2. Besides, an initial state assignment SA_0 using state variables (x, y, z) is scheme I in Table 3 with state set $S=\{A,B,C,D,E,F\}$ and redundant state set $RS=\{100,101\}$.

Table 2: state of corrector

Present state	Next state $T=0$	Next state $T=1$	Output R $T=0$	Output R $T=1$
A	*B*	*B*	0	0
B	*C*	*D*	0	0
C	*E*	*F*	0	0
D	*F*	*F*	0	0
E	*A*	*A*	0	0
F	*A*	*A*	0	1

Table 3: state assignment

State	Scheme I x	Scheme I y	Scheme I z	Scheme II x	Scheme II y	Scheme II z
A	0	0	0	ϕ	0	0
B	0	0	1	ϕ	0	1
C	1	1	1	1	1	1
D	0	1	1	0	1	1
E	1	1	0	1	1	0
F	0	1	0	0	1	0

From this state assignment the excitation functions of three flip-flips and the output function are:

$$D_x = \overline{T}xz + \overline{T}\overline{y}z,$$

$$D_y = z,$$
$$D_z = \bar{y},$$
$$R = T\bar{x}y\bar{z}. \quad (3)$$

Now we discuss the multi-code assignment using algorithm 1.

Step 1: Because RS is not empty, define $\mathrm{SA}_{\mathrm{temp}}$ to be SA_0 and compute the occurrence probabilities of all the states in S based on Table 2 as follows.

Suppose a, b, c, d, e, f are occurrence probabilities of the six states *A, B, C, D, E, F*, and τ is the probability of input variable $T = 1$. In line with the relationship between the present state and the next state, we have probability equalities as follows.

$$\begin{aligned} a &= e + f \\ b &= a \\ c &= b \cdot (1 - \tau) \\ d &= b \cdot \tau \\ e &= c \cdot (1 - \tau) \\ f &= c \cdot \tau + d \end{aligned} \quad (4)$$

Take the first equality in eqn.4 as example, from Table 2 we find that the next state will be *A* if, only if the present state is *E* or *F*, thus $a = e + f$ is obtained. Other equalities in eqn.4 are obtained analogously. Due to eqn. 4, we have

$$a = b = c + d = e + f \quad (5)$$

Furthermore, according to the normalization of probability values, we have:

$$a + b + c + d + e + f = 1 \quad (6)$$

Suppose τ is 0.5, we have $a = b = 25\%$, $\mathrm{c} = \mathrm{d} = 12.5\%$, $\mathrm{e} = 6.25\%$ and $\mathrm{f} = 18.75\%$. Therefore, S is sorted as $\mathrm{S} = \{\mathrm{A}, \mathrm{B}, \mathrm{F}, \mathrm{C}, \mathrm{D}, \mathrm{E}\}$ in descending order of probabilities.

Step 2: For the first state A in S, cube $\bar{y} \cdot \bar{z}$ covers its code “000” and one redundant state “100”. Furthermore, it is the largest cube since either $\bar{\mathrm{y}}$ or $\bar{\mathrm{z}}$ covers other states in S. Hence two codes, “000” and “100” are assigned to state A and remove “100” from the redundant state set. Thus RS becomes {101} with only one redundant state. For the next state B in S, cube $\bar{y} \cdot z$ is the largest cube that covers “001” and the only left redundant state “101”. Therefore two codes “001” and “101” are assigned to state B and RS is empty now.

Step 3: The result in step 2 gives another scheme SA_1 which is shown as scheme II in Table 3.

The excitation functions of flip-flops and the output function using SA_1 can be extracted as

follows:

$$D_x = \overline{T}x + \overline{T}\overline{y}$$
$$D_y = z \qquad (7)$$
$$D_z = \overline{y}$$
$$R = T\overline{x}y\overline{z}$$

Compared the above equation with eqn.3, D_y, D_z and R are the same, D_x is clearly simplified and consequently needs less power dissipation. Therefore, update $\mathrm{SA}_{\mathrm{temp}}$ with SA_1. In step 2, cubes $\overline{y} \cdot \overline{z}$ and $\overline{y} \cdot z$ are unique cube selection for states A and B respectively. In other words, there is no alternative selection of cubes for these two states. So go to step 4.

Step 4: Because $\mathrm{SA}_{\mathrm{temp}}$ and SA_0 are different replace SA_0 with $\mathrm{SA}_{\mathrm{temp}}$ and go to step 1 of algorithm 1.

Step 5: In step 2, RS is reduced to be empty. Hence just return the updated SA_0 that is scheme II in Table 3 as the final state assignment and exit.

With the new scheme obtained from example 2, it can be seen that when the system is in state A or state B, $y = 0$ can be used to isolate the clock which triggers flip-flop x so as to save 50% of the flip-flop's energy dissipation. As to all three flip-flops, the energy dissipation saving is about 16.7%.

4 Conclusions

Since state assignment in design of sequential circuits influences the complexity of combinational circuit, people attach importance to it all long in the traditional design. In the low power design, we find that the procedure of state assignment influences the state signal's switching behavior during the state switching process. As the input to the combinational circuit, state variable lines have a close relation with the system's energy dissipation. Thus state assignment is an important research topic in low power design. Previous research has resulted in low power state assignment that would assign codes with minimum Hamming distances to states with high transition probabilities. This paper in contrast proposed state assignment that would exploit the redundant state codes to gate the clock to some of the flip-flops. Multi-code state assignment not only eliminates the redundant state codes but also improves the system's reliability. An algorithm is hitherto proposed for the multi-code state assignment and three practical design examples show that this technique is feasible and can reduce energy dissipation.

5 Acknowledgment

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