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A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages

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SUMMARY

In this paper, a SRAM cell structure which uses pMOS access transistors and predischarged bitlines is presented. By using the strained pMOS transistor technology, the degradation of the read static noise margin (SNM) at high supply voltages due to the aging, especially in the presence of symmetric stress, is suppressed. In contrast to conventional cell, the write margin of the proposed cell does not degrade considerably at low supply voltages. To assess the efficacy, the proposed cell is compared with conventional cell for two cases of unstrained and strained pMOS. A comparative study is performed using mixed mode device/circuit simulations for a gate length of 22 nm. The results show that the read SNM degradation due to the symmetric aging at the supply voltage of 1 V is about 6% after three years for the proposed strained structure, while degradations are 14%, 12%, and 11% for the unstrained proposed structure, unstrained, and strained conventional structures, respectively. In addition, the proposed cell has both read and write cell sigma yields higher than six for supply voltages ranging from 1 V down to 0.5 V while the other structures have read or write yields less than six at the minimum supply voltage. Through some work function tuning, the cell sigma yields of the other structures reach above six for both read and write while being still lower than those of the proposed structure. Copyright © 2015 John Wiley & Sons, Ltd.

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KEY WORDS: minimum operating voltage; NBTI; PBTI; SiGe S/D; SRAM; yield

1. INTRODUCTION

Normally, SRAM cells are composed of minimum-sized transistors suffering from short channel effects and process variations. The latter occurs due to variations in the physical parameters of the device such as the channel doping and length yielding variations in the device characteristics. As a result the stability and the performance of SRAM cells are considerably degraded. To overcome these problems, conventional bulk transistors have been replaced by FinFET where a better control of short channel effects and a higher immunity against the process variation can be achieved [1]. The improvements originate from the strong gate electrostatics control and lightly doped thin film body, respectively. In addition, using high-k gate dielectric further reduces the short channel effects and also gate leakage current [2].

In addition, changes in the characteristics of the transistors may occur over time [3]. This temporal variability is mainly due to Bias Temperature Instability (BTI) which increases the magnitude of the threshold voltage of the devices, and hence, adversely affects the performance [4]. For pMOS (nMOS) transistors, the effect occurs under negative (positive) bias and hence is called NBTI

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(PBTI). The problem becomes even worse as the technology scales further. Because as the channel length and gate oxide thickness are scaled, due to some reliability concerns operating voltages cannot be scaled as much [5]. This results in creation of higher electric field intensities in the gate oxide aggravating the BTI. The BTI effect, in turn, degrades the performance of integrated circuits [6].

The NBTI problem is minimized when the pMOS channel is under stress as is in the case of strained pMOS originally suggested for improving the mobility [7]. The common approach for inducing the strain in pMOS is the use of SiGe alloy for the source and drain of the transistor. Due to the larger lattice constant of SiGe compared to that of Si, a compressive stress is produced in the channel, thereby improving the hole mobility [8]. The same approach may be used in FinFET [9, 10]. In this work, we present an SRAM cell structure making use of strained pMOS to improve the robustness against the BTI. The proposed cell also has a high yield for low V_{dd}'s where the BTI problem is of less concern. The rest of the paper is organized as follows. The device considerations are presented in section 2, and some of the related works are discussed in section 3, while section 4 describes the proposed SRAM cell structure. In section 5, the results are presented and discussed. Finally, section 6 concludes the paper.

2. DEVICE CONSIDERATION

We use a 22-nm double-gate FinFET technology with parameters similar to those used in [11] (see Table I). Similar to [11], we assume a single gate material (near midgap) for both nMOS and pMOS providing us with strictly packed transistors. It should be noted that this assumption should not affect the results of the comparative study presented in section 5. The 2D simulations are performed using the device and process simulators of Silvaco, namely Atlas and Athena, respectively [12], assuming that the top gate does not have any control over the channel due to the higher oxide thickness. The high field mobility model CVT is used in our simulations. The coefficients of the model are calibrated using the experimental data presented in [13, 14]. The results of the *I–V* characteristics are in very good agreement with those presented in [11].

To enhance the transistor mobility, some techniques such as contact etch stop layers (CESL) and SiGe source/drain may be used [10]. However, CESL is not as effective as using SiGe source/drain and is not practical in some FinFET processes [10]. Hence, we ignore this kind of straining. But, to take advantage of the robustness against NBTI, the promising method of using embedded SiGe source/drain p-channel FinFET structure is used [9, 10]. In this work, we assume that the alloy used is $Si_{0.6}Ge_{0.4}$. The magnitude of the initial stress for process simulations was found from [10]

$$S_{ii} = \frac{E}{1 - 2\,.\,v} . \frac{a_{Si} - a_D}{a_{Si}} \,.D\% \tag{1}$$

where i is a Cartesian coordinate (x, y, or z), E is the Young modulus for silicon, υ is Poisson's ratio for the channel direction that is found from [15], a_{Si} and a_D are the lattice constants of silicon and embedded materials (germanium here), respectively, and $D\%$ is the percentage of the embedded impurity (40% in our case). After recess etching of the source/drain and recovery of stress, a stress relaxation in the channel occurs creating a non-uniform smooth distribution profile for the stress. It should be noted that our final (after stress relaxation) channel stress profile was similar to that of [10].

Table I. Device parameters used for simulations.

Channel length, L_g (nm)	22
Equivalent oxide thickness, t_{oxe} (A°)	11
Fin thickness, t_{si} (nm)	15
Channel doping, N_{body} (#/cm^{-3})	10^{16}
Fin height, H_{fin} (nm)	30
Gate work function (eV)	4.65

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In Figure 1, the current versus gate voltage (I_d–V_g) characteristics obtained from device simulations are plotted. For the linear region ($|V_{ds}|=0.1$ V), the strained pMOS has a smaller slope for the I_d–V_g characteristics than the unstrained one at high $|V_{gs}|$ values leading to partial compensation of the NBTI [16]. The smaller proportionality of the drain current with the gate voltage is due to more mobility (μ_{eff}) degradation with the increase in the vertical electric field (E_{eff}) in the case of short channel strained pMOS [7]. The strain reduces inter-valley phonon scattering leaving surface roughness scattering (which has a steeper negative slope for the μ_{eff}–E_{eff} characteristic) as the dominant component [7,16]. In other words, at high $|V_{gs}|$ values, with increasing $|V_{gs}|$ and consequently E_{eff}, the mobility decreases more for the strained pMOS with respect to the unstrained one, resulting in a smaller slope for the I_d–V_g characteristics. The smaller slope corresponds to a smaller proportionality coefficient for the relation between I_d and $(|V_{gs}|-|V_{th}|)$. Thus, the effect of the threshold voltage change due to NBTI influences the current less than that of the unstrained device in the linear region. In the saturation region, the compensation of NBTI disappears [16]. In the case of strained nMOS, the slope of μ_{eff}–E_{eff} is not much different than that of the unstrained one, and hence the slopes for the I_d–V_g characteristics are about the same [8].

The threshold voltage increase ($\Delta V_{th-static}$) due to the BTI effect may be obtained from [17]

$$\Delta V_{th-static} = \frac{qN_{it}}{C_g} \tag{2}$$

where q is the electric charge, N_{it} is the trap densities (due to NBTI or PBTI), and C_g is the gate capacitance. The term static in the subscript denotes the fact that the stress signal is time invariant. If the stress signal varies by the time, the dc (static) degradation should be multiplied by a prefactor so as to consider the signal (stress) probability. The simplified ac model for the threshold voltage shift over time is given by

$$\Delta V_{th-ac} = \alpha \Delta V_{th-static}. \tag{3}$$

where α is a function of signal probability (e.g. 0.796 for a duty cycle of 50%) while fairly independent of the frequency [18]. The total time duration considered in this work is 1×10^8 s. Also, the trap densities for high-k after 1×10^8 s (BTI stress time considered in this work) for typical surface orientation of (110) are extracted from Table I of [17] for $V_{dd}=1$ V. It should be noted that since there was no published report on BTI data for SiGe source/drain FinFETs, we used BTI degradation results presented in [17]. It was shown in [19] that the strain (embedded SiGe as source/drain) did not create conditions for additional trap density generation by the BTI for a given oxide electric field obtaining the same BTI degradation effects.

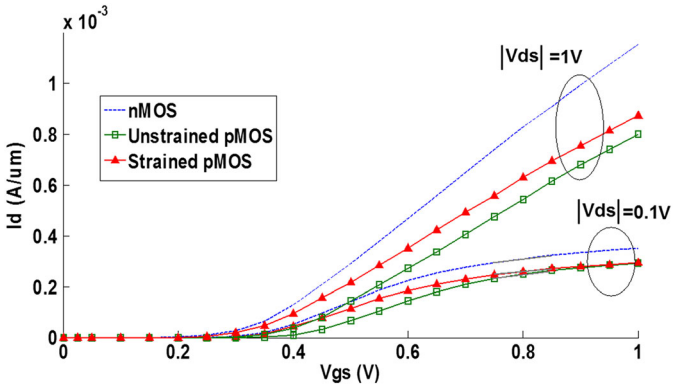

Figure 1. I_d–V_g characteristics for strained and unstrained pMOS and nMOS structures for linear region ($|V_{ds}|=0.1$ V) and saturation region ($|V_{ds}|=1$ V).

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3. RELATED WORKS: CONVENTIONAL AND MODIFIED STRUCTURES

In this section, first, we present a brief analysis for the read and write stabilities of the conventional structures. Also, the effect of symmetric and asymmetric stresses on these parameters is provided. Then, a review of the effect of straining on the stability of the conventional structure and the modified structures for mitigating the effect of BTI and improving the stability are presented.

3.1. Conventional structure

A conventional 6-T SRAM cell shown in Figure 2(a) is referred to as AXN in this work. The most important parameter of the SRAM cells that degrades due to the BTI is the read stability as has been shown in the literature (see, e.g. [18,20]). For this cell, during the read operation, first the bitlines are precharged to V_{dd}, and then the wordline is asserted. In this case where the cell has stored '1' (VL = '1'), VR rises to $V_{\text{read-n}}$ (where subscript n indicates using nMOS access). If $V_{\text{read-n}}$ becomes greater than the trip voltage of the inverter PL–NL, which is denoted by $V_{\text{trip-n}}$, the cell state will flip and a read failure will occur. Neglecting OFF state current of transistors, $V_{\text{read-n}}$ and $V_{\text{trip-n}}$ were found in [21] by solving the following equations:

$$I_{\text{Dsat}-\text{AR}}\left(V_g = V_{dd}, V_s = V_{\text{read}-\text{n}}, V_d = V_{dd}\right) = I_{\text{Dlin}-\text{NR}}\left(V_g = V_{dd}, V_s = 0, V_d = V_{\text{read}-\text{n}}\right) \tag{4}$$

$$\begin{aligned} &I_{\text{Dsat}-\text{NL}}\left(V_g = V_{\text{trip-n}}, V_s = 0, V_d = V_{\text{trip-n}}\right) \\ &\quad = I_{\text{Dsat}-\text{PL}}\left(V_g = V_{\text{trip-n}}, V_s = V_{dd}, V_d = V_{\text{trip-n}}\right) \\ &\quad + I_{\text{Dsat}-\text{AL}}\left(V_g = V_{dd}, V_s = V_{\text{trip-n}}, V_d = V_{dd}\right). \end{aligned} \tag{5}$$

Here, $I_{\text{Dsat-X}}$ and $I_{\text{Dlin-X}}$ are the drain currents of the transistor X in the saturation and linear regions, respectively.

For the BTI degradation, we consider two cases of asymmetric and symmetric stresses. In the former case, a cell stores the same data for a long time resulting in a deterioration of only two devices in the cross-coupled inverters (e.g. NR and PL in Figure 2). In the latter case, data is regularly flipped between the two storage nodes of the cell leading to the degradation of all four devices in the cross-coupled inverters. It should be noted that, in all the structures, since the access transistors are OFF most of the times, their performances are not affected by the BTI effect and only the pull-up and pull-down transistors are affected. As discussed in [20], if the cell stores '1' for a long time (asymmetric stress), NR and PL will suffer from the degradation due to PBTI and NBTI causing increases in the absolute values of their threshold voltages, respectively. This leads to the increment in $V_{\text{read-n}}$ (e.g. 8.7% for the strained structure at V_{dd} = 1 V) and decrease in $V_{\text{trip-n}}$ (5.8%), respectively, reducing the read stability. In the case of symmetric stress, all four transistors of the back to back inverter degrade by a constant coefficient. In this case, $V_{\text{read-n}}$ increases (6.5%) less than that of the asymmetric stress due to the less degradation of NR after the symmetric stress (50%

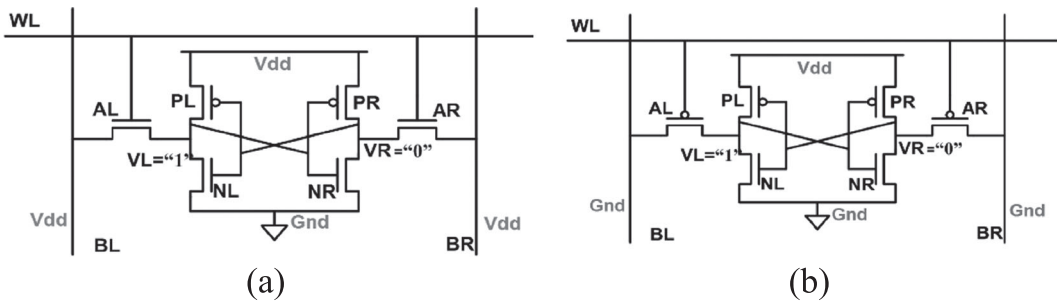

Figure 2. Schematics of (a) a conventional 6-T SRAM cell with nMOS access and precharged bitlines (AXN) and (b) the proposed SRAM cell with pMOS access and *predischarged* bitlines (AXP).

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duty cycle) compared to that of the asymmetric stress case (100% duty cycle and hence two times more stress time), and $V_{\text{trip-n}}$ remains relatively unaltered as both NL and PL degrade (2.5% increase for the strained structure at $V_{dd} = 1$ V). Thus, the read stability degradation is reduced for the symmetric stress with respect to the asymmetric stress as the PBTI effect compensates the NBTI for $V_{\text{trip-n}}$ and the PBTI effect on $V_{\text{read-n}}$ is lowered. It is worth mentioning that the symmetric stress is practically possible using some methods presented in the literature (see, e.g. [22, 23]).

To write a '1' into the cell that stores '0' (Figure 2), the voltage of BL (BR) is set to 0 (V_{dd}), and then the wordline is asserted. In this case, for the AXN structure (Figure 2(a)), the left node (L) is discharged through AL. If VL, which is determined by the voltage division between PL and AL, becomes lower than the trip voltage of PR and NR ($V_{\text{trip-n}}$), the write operation will be performed. As discussed in [20], the write stability improves in the presence of a symmetric stress as the stress weakens the back to back inverter feedback loop making it easier to break. After asymmetric stress, degradations of PL and NR make discharging the node L and charging the node R easier, and also increase $V_{\text{trip-n}}$ for the conventional (AXN) structure. These changes lead to a higher write stability for the asymmetric stress case. In [24], the worst case for the write operation has been considered where the cells have stored '0' initially for a long time. For this situation, the degradations occur for PR and NL (instead of PL and NR). Then, we may assume that we perform a *first* write by storing '1' in the cells and instantly performing the *second* write aiming to restore the original state of '0'. For the second write, $V_{\text{trip-n}}$ decreases, and charging node R remains unaffected. Thus, there is a write stability degradation in this case [24].

3.2. *Modified structures*

The results presented in [16,25] confirm that the cells with strained pMOS are more robust against the NBTI during the read operation. The improvement, however, is marginal because only PL (in Figure 2) experiences the NBTI degradation reducing the read stability. However, PL determines $V_{\text{trip-n}}$ while working in the saturation region (see 5). Hence, as discussed in section 2, a considerable compensation of the NBTI effect is not achieved [25]. Other techniques such as dynamic body biasing can improve the initial and after BTI degradation characteristics of the SRAM cell [26, 27]. The improved characteristics include the read and write stabilities and speeds [26, 27]. The area and power penalty of these techniques, however, are noticeable [26, 27].

To improve the cell stability, a departure from the conventional 6-T cells by increasing the transistor numbers has been suggested in the literature (see, e.g. [28]). The approach, however, increases the area of the cell and consequently the area of the memory part of the chip. To increase the read and write stabilities of FinFET SRAM cells without increasing the area, static and dynamic back-gate designs have also been proposed [21,29]. The back-gate design requires implementing both independent-gate and tied-gate double gate FinFETs on the same die [29]. Using the independent gate structure, high yield 4-T FinFET SRAM cells have also been suggested in [30]. The driverless 4-T cell combines the task of the pull-down and access transistors using one independent gate nMOS. In this cell, logic '0' is preserved by connecting the back-gate of the access transistors to the opposite storage nodes and predischarging the bitlines to zero. The use of pMOS access transistors for increasing the read stability of FinFET SRAM cells has also been suggested in [31]. In this work the conventional approach of precharging the bitlines is used.

4. PROPOSED STRUCTURE

In this paper, we propose using pMOS access with the bitlines *predischarged* during the read and hold states similar to driverless 4-T SRAM cells discussed in [30]. The cell, which is shown in Figure 2(b), is called AXP. In this case, for the read operation, WL is asserted (grounded), and the read operation is performed by charging the BL line through the transistor AL (see Figure 2(b)). When the difference between BL and BR levels reaches a certain value (e.g. $0.1V_{dd}$), the sense amplifier operates to complete the read operation. In this operation, VL decreases to $V_{\text{read-p}}$ (where the subscript p indicates using pMOS access). If $V_{\text{read-p}}$ is less than the trip point of PR-NR denoted by $V_{\text{trip-p}}$, a

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read failure will occur. Neglecting OFF state current of the transistors, $V_{\text{read-p}}$ and $V_{\text{trip-p}}$ can be found from the following equations:

$$I_{\text{Dsat}-\text{AL}}\left(V_g = 0, V_s = V_{\text{read}-\text{p}}, V_d = 0\right) = I_{\text{Dlin}-\text{PL}}\left(V_g = 0, V_s = V_{dd}, V_d = V_{\text{read}-\text{p}}\right) \tag{6}$$

$$\begin{aligned} &I_{\text{Dsat}-\text{PR}}\left(V_g = V_{\text{trip}-\text{p}}, V_s = V_{dd}, V_d = V_{\text{trip}-\text{p}}\right) \\ &\quad = I_{\text{Dsat}-\text{NR}}\left(V_g = V_{\text{trip}-\text{p}}, V_s = 0, V_d = V_{\text{trip}-\text{p}}\right) \\ &\quad + I_{\text{Dsat}-\text{AR}}\left(V_g = 0, V_s = V_{\text{trip}-\text{p}}, V_d = 0\right) \end{aligned} \tag{7}$$

It should be noted that only PL experiences NBTI degradation reducing the read stability. In our proposed structure, due to using the *prediscbarged* bitlines, the degraded PL is involved in the V_{read} calculation while working in the linear region with high $|V_{gs}|$ (see 6). Thus, one would expect that the use of the strained pMOS would reduce the aging effect on $V_{\text{read-p}}$ lowering the read stability degradation (see section 2). As discussed in section 3, the same compensation of NBTI may not be achieved in the conventional cell (AXN) as PL determines $V_{\text{trip-n}}$ while working in the saturation region (see 5).

For the case of asymmetric stress, due to NBTI, PL becomes weak lowering $V_{\text{read-p}}$. Also, PBTI degrades NR enlarging $V_{\text{trip-p}}$ and in turn, degrading the read stability. For the symmetric stress case, similar to the conventional structure, we expect a lower change in $V_{\text{read-p}}$ (due to less NBTI effect) and almost no change in $V_{\text{trip-p}}$ (due to the compensation of the PBTI effect by the NBTI effect) reducing the read stability degradation.

During the write operation, in our proposed AXP structure (write '1' in Figure 2(b)), the right node (R) is charged through AR. If VR, which is determined by the voltage division between NR and AR, becomes higher than the trip voltage of PL and NL ($V_{\text{trip-p}}$), the write operation will be performed. With a similar discussion for the conventional structure, the symmetric stress improves the write stability, and marginal degradation can occur in the worst case second write.

5. RESULTS AND DISCUSSION

To assess the efficacy of the proposed SRAM cell, we compare the characteristics of the SRAM cells with nMOS access shown in Figure 2(a) (AXN, Strained AXN), and our proposed cells with pMOS access transistors shown in Figure 2(b) (AXP, Strained AXP). Only the strained structures make use of strained pMOS. In this work, from now on, we denote Strained AXN and Strained AXP as SAXN and SAXP, respectively. Next, we study the parameters of one SRAM cell in each structure obtained from mixed mode device/circuit Silvaco (Atlas) simulations [12]. We also show the impact of supply voltage scaling (0.5–1 V) on the characteristics of the SRAM structures. The generated trap densities due to BTI for the supply voltages of 0.5–0.9 V were approximated from the analytical expression given in [32]. We used the experimental results presented in [17] for the (110) surface orientation at $V_{dd} = 1$ V to find the fitting parameters of the model. Also, it should be noted that the band structure is affected by the strain modifying the threshold voltage and the oxide electric field. These oxide electric fields should be used in the model to obtain the BTI results. Figure 3 shows the trap densities and the threshold voltage shifts (using 2 and 3) resulted from the BTI effect after asymmetric stress (solid) and symmetric stress (dotted) time of 1×10^8 s versus V_{dd}. The results include strained pMOS, unstrained pMOS, and nMOS structures. As expected both the trap densities and threshold voltage shifts monotonically increase when the supply voltage increases. The lower threshold voltage shift for the symmetric case originates from the coefficient of α which was less than 1 (see 3). It also should be noted that the strained pMOS transistor has a slightly higher threshold voltage shift than the unstrained one (see Figure 3(b)). This slight increase in the shift,

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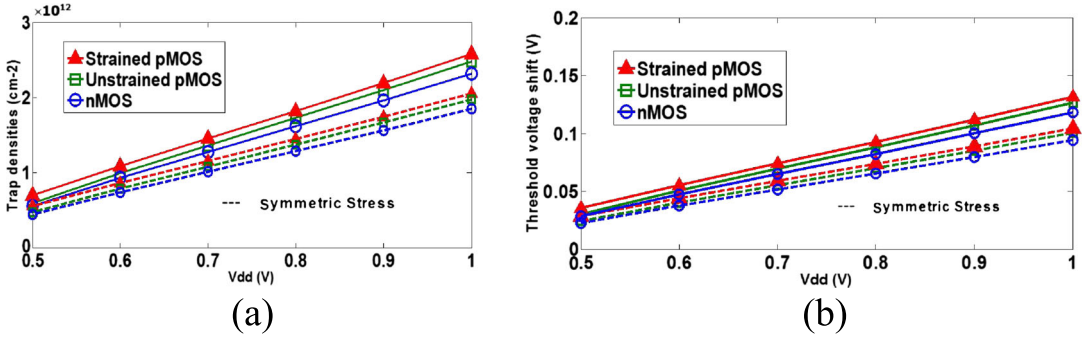

Figure 3. (a) Interface trap density and (b) threshold voltage shift after asymmetric stress (solid) and symmetric stress (dotted) versus V_{dd} for strained and unstrained pMOS and nMOS structures. The stress time was assumed to be 1×10^8 s.

however, does not lead to more decrease in the drain current due to the smaller slope of I_d–V_g characteristic for this structure (see section 2).

5.1. *Nominal study*

Read static noise margin (SNM) is the widely used read stability criterion [33]. It can be quantified by the length of the side of the maximum square that can fit inside the butterfly curves. The butterfly curves are obtained by sweeping the storage node voltages from zero to V_{dd} during the read operation. It should be noted that during the read operation, the bitlines and wordline are set to V_{dd} for the conventional structures (AXN and SAXN), while they are set to zero for our proposed structures (AXP and SAXP). Figure 4 shows the read SNM values obtained from the mixed mode device/circuit simulations for different structures. Compared to the case of unstrained transistors, the use of strained pMOS increases the read SNM of the conventional AXN cell. The increase in the case of the SAXN is due to the stronger pMOS and larger $V_{\text{trip-n}}$. As a result of the NBTI/PBTI, the read SNM degrades 12% (11%) and 50% (44%) for AXN (SAXN) after symmetric and asymmetric stress cases at $V_{dd} = 1$ V, respectively (see section 3). The lower degradations of the SAXN may be due to the more resistance of the strained transistors towards aging as was also observed in [7]. We, however, should note that compared to the case of AXP, the use of strained pMOS decreases the read SNM of the SAXP. This originates from the increase in $V_{\text{trip-p}}$ (due to the strengthened pMOS) which in turn leads to a less read stability (see the discussion in section 4). To make the read SNM of the cell acceptable, we increase $V_{\text{read-p}}$ by augmenting the fin number of the pull-up transistors to two. Using this strategy, the read SNM of the SAXP became larger than that of the AXP. This increase, however, deteriorates the write stability by about the same amount (see Figure 6 in [11]). Since, the write margin of SAXP is high enough in the one fin cell, its decrease due to fin number increases does not make its value unacceptably low with voltage scaling (see Figure 7(a)). In the

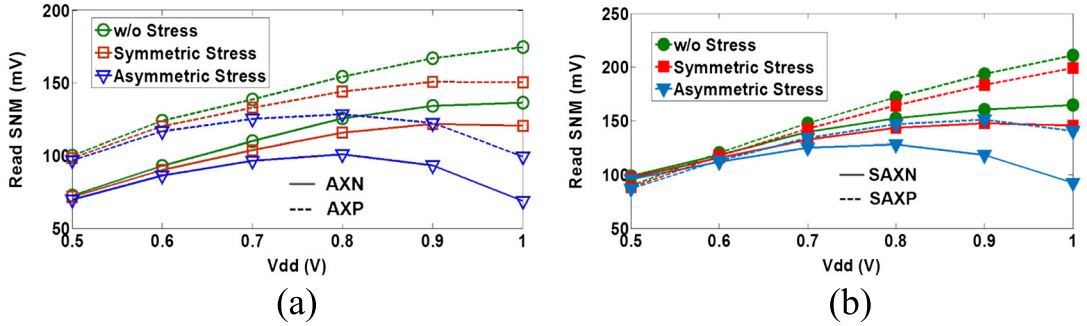

Figure 4. Nominal read SNM versus V_{dd} for (a) unstrained and (b) strained AXN (line) and AXP (dotted) structures. The stress time was assumed to be 1×10^8 s.

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case of other structures, write stabilities are noticeably degraded with the supply voltage scaling, and hence, using the similar sizing causes further deteriorations of their write stabilities especially at low supply voltages. In addition, this sizing does not have any impact on the area if the spacer pattern technology is used [34] (see Figure 5). In this technology, the fins are formed using spacer layers deposited around a sacrificial layer. The technology provides even number of fins. One of the fins is etched away if odd numbers of fin is required. Figure 5 shows the layout of different structures. Similar to [35], the layout has been drawn based on the analysis given in [36]. For the SAXP, at $V_{dd} = 1$ V, after an asymmetric stress, the read SNM decreases 33% while the degradation is 43% for the AXP. For the symmetric stress case, the aging has a smaller impact on the read SNM (6% and 14% for SAXP and AXP, respectively) as we expect (see section 4). Moreover, the SAXP structure is more robust against the symmetric BTI than the SAXN (6% versus 11% degradation). This is due to the compensation of NBTI for $V_{\text{read-p}}$ of SAXP as discussed in section 4. For the asymmetric stress case, the compensation of NBTI for $V_{\text{read-p}}$ decreases as $V_{\text{read-p}}$ decreases more and PL approaches the saturation region. We also demonstrate that the evolution of read SNM over time in Figure 6 which reveals the degradation of the SAXP structure under the symmetric stress is the least compared to those of the other structures.

The results presented in Figure 4 show the impact of supply voltage scaling on the characteristics of the SRAM structures. As it is expected, in without stress and after the symmetric stress cases, the read SNM decreases with lowering V_{dd}. The highest reduction is for the SAXP, while the lowest reduction belongs to the SAXN. This may be attributed to the fact that the strength ratio of the strained pMOS with respect to the unstrained one becomes more with the supply scaling (see Figure 1). Thus, V_{trip} decreases less for the strained pMOS structures with the scaling. This suppresses the read SNM degradation for the SAXN while making worse the degradation for the SAXP. After an asymmetric stress, at high V_{dd}'s, the read SNM first increases when V_{dd} is lowered and then starts to decrease.

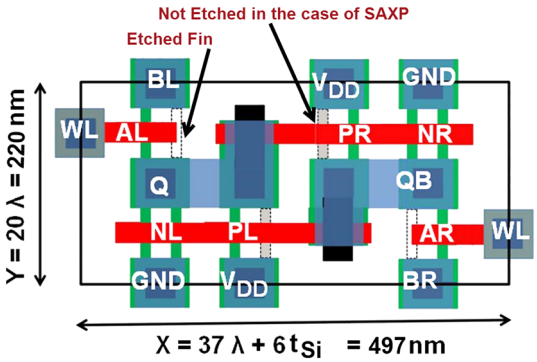

Figure 5. Thin-cell layout of structures [35]. AL and AR are nMOS in the case of AXN (SAXN), while they are pMOS in the case of AXP (SAXP). For all the transistors, one of the fins has been etched away except for the pull-up transistors in the SAXP which have two fins.

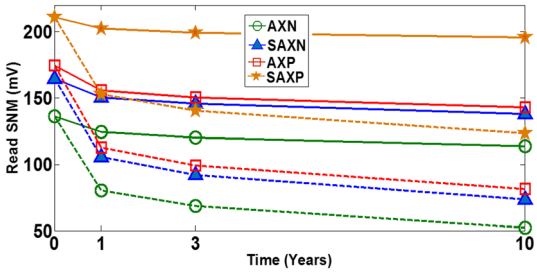

Figure 6. Nominal read SNM versus time for different cells at $V_{dd} = 1$ V for the cases of symmetric (line) and asymmetric stresses (dotted).

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The initial increase indicates that when V_{dd} becomes smaller, the reduction in the BTI due to the lower electric field is more effective than the decrease in the SNM by decreasing the supply voltage. When the supply voltage reduces further, the read SNM becomes lower with the V_{dd} scaling showing that the latter effect is the dominant one.

Another important metric in the read state is the access time for which the read current is used as a measure [11]. The read current is the current of the access transistor whose source voltage is $V_{\text{read-n}}$ ($V_{\text{read-p}}$) for AXN and SAXN (AXP and SAXP) structures during the read state. Figure 7(a) shows the read currents for different structures at $V_{dd} = 1$ V. As the results show, using the strained pMOS transistors slightly decreases the read current for the conventional AXN structure. The reason is that the strained pull-up transistor has a higher leakage current, which increases V_{read} slightly, consequently reducing the read current (it should be noted that the OFF state current of the pull-up transistor has been neglected in 4). Although the AXP cell structure has less read current than the AXN and SAXN, SAXP structure has the highest read current. The reason is that due to using two fin pull-up transistors, $V_{\text{read-p}}$ becomes high, increasing the overdrive of the access transistors during the read operation. For this structure, NBTI/PBTI causes the least reduction ratio in the read current as the change in V_{read} is the minimum. Also, as asymmetric stress does not alter V_{read} very much with respect to the symmetric stress, read current decreases only a little more after the asymmetric stress. Next we study the impact of the supply voltage on the read current. It should be noted, the stress has a negligible impact on the read current (see Figure 7(a)), and hence, the read currents after applying the stress are not presented here. The dependence of the read current versus the supply voltage is plotted in Figure 7(b) which shows that the current decreases linearly with lowering V_{dd}. The linear dependence of the saturation current originates from the velocity saturation in the transistors in these technologies.

To compare the write characteristics of the SRAM structures, the combined word line margin (CWLM) metric was evaluated due to its normal distribution in the presence of process variations [37, 38]. CWLM is defined as a difference between V_{dd} and the minimum wordline voltage that can cause a successful write operation [37]. As discussed in section 3, the write margin increases in the cases of the symmetric stress and asymmetric stress for the first write. Thus, we only present the results of the initial and the asymmetric stress when the worst case condition (i.e. second write) occurs. As shown in Figure 8, the degradation is marginal in the worst case condition. Also, the strain increases the write margin of the proposed SAXP structure due to the strengthening of the pMOS access transistor. In the case of the SAXN structure, the strain decreases the write margin because it strengthens the pull-up which competes with the access transistor during the write operation. The figure also reveals that the write margins for all the structures decrease with lowering V_{dd}. In the case of the proposed SAXP structure, the reduction is negligible indicating a low sensitivity to V_{dd}. This is due to the fact that with lowering V_{dd}, the relative reduction in the strength of the strained pMOS access transistor is less than that of the competing pull-down during the write operation. Finally, note that the static powers of all the structures (including the proposed SAXP with two fins pull-up) for all the

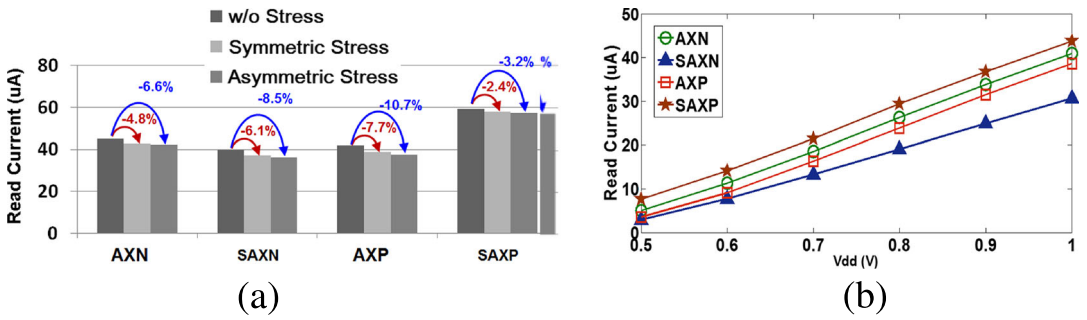

Figure 7. (a) Nominal read current for different structures at $V_{dd} = 1$ V (stress time was assumed to be 1×10^8 s) and (b) nominal read current versus V_{dd} in without stress case.

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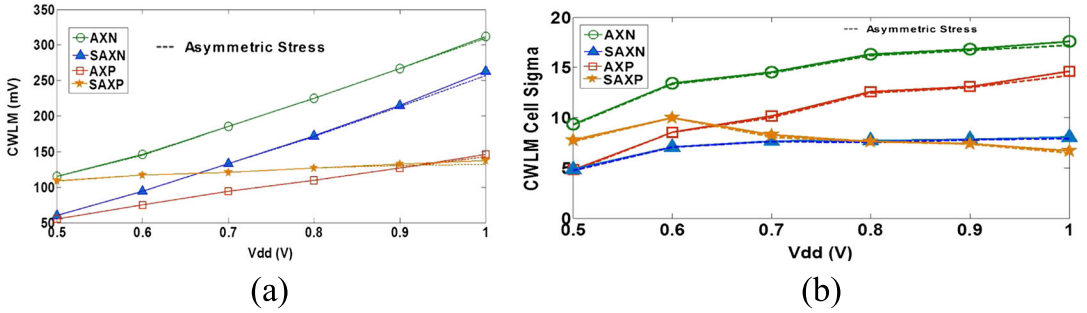

Figure 8. (a) Nominal CWLM value and (b) CWLM cell sigma versus V_{dd} for different cells for the cases of without stress (line) and after asymmetric stress (dotted).

supply voltages were below 10 nW per cell (due to using a near midgap workfunction). It should be noted that in the hold state, for the proposed structures, the wordline is V_{dd} while the bitlines are predischarged to zero. In this state, for the conventional structures, the wordline is zero, while the bitlines are precharged to V_{dd}. For the two cases, the access transistors (nMOS and pMOS for the conventional and proposed structures, respectively) are OFF consuming about the same leakage powers (all below 10 nW). In the case of the dynamic power, for each read or write operation, the wordline should be activated and then deactivated to come back to the hold state. Since the dynamic power is drawn from the supply voltage only during the zero to one transition and the number of these transitions is the same for all the structures, the power consumptions should be the same for all these structures. Note that, as has been shown in Figure 5, the proposed and conventional structures have the same areas and therefore the same capacitive loads (mainly determined by the bitline interconnect length [5]) for a given data volume. With a similar reasoning the bitline voltage changes for the structures consume the same dynamic power.

5.2. *Investigation of the process variation effect*

Now, we study the impact of the process variation on the SRAM cell structures discussed in this work. Among different sources of variations the random dopant fluctuation can be ignored due to the lightly doped body. The variations of the fin height and oxide thickness whose values are not determined by lithography conditions are also not critical (see, e.g. [39]). Channel length and silicon thickness are the main parameters subject to the process variations (see, e.g. [11,21,39]). The experimental results presented for the FinFET variations have shown that only considering the two parameters would be sufficient [39]. It should be mentioned that including other variation sources may be readily performed by extending the analysis given below. For the process variation study, we assume that the channel length (L_g) and the silicon thickness (t_{si}) have the Gaussian distribution [11]. The variations can be divided into local and global variations. The local variations are uncorrelated ($r=0$, which r is the correlation coefficient), while the global variations of the neighboring transistors are assumed to be completely correlated ($r=1$) [39]. The local and global variances of L_g and t_{si} are estimated to be $3\sigma=10\%$ of their nominal values. This estimation is derived from the data reported in [39]. We present the variability of each transistor by considering local and global variations of both L_g and t_{si}. This leads to four variables for each of the six transistors and 24 random variables for the whole cell. Among them, 12 variables represent local variations and 12 variables represent global variations of L_g and t_{si}. Read SNM and CWLM are very well modeled with normal distributions [37, 38]. Therefore, we assume that the metrics have Gaussian distributions which are related to the random variables via a function. Denoting the metric by y, we may write

$$y = f(x_1, \ldots, x_{24}). \tag{8}$$

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where $x_1,\ldots,x_{24}$ are the random variables with averages of $\eta_1,\ldots,\eta_{24}$ and standard deviations of $\sigma_1,\ldots,\sigma_{24}$. Let us denote the correlation coefficient between x_i and x_k by r (i,k). Hence, we can use the following expressions to find their statistical characteristics using bivarient Taylor Series as [40]

$$\mu_y = f(\eta_1, \ldots, , \eta_{24}) \tag{9}$$

$$\sigma_y^2 = \sum_{i=1}^{24} \left(\frac{\partial f}{\partial x_i}\bigg|_{\eta_i} \right)^2 \sigma_i^2 + 2 \sum_{k=1}^{24} \sum_{i=1;i\neq k}^{24} \left(\frac{\partial f}{\partial x_i}\bigg|_{\eta_i} \right) \left(\frac{\partial f}{\partial x_k}\bigg|_{\eta_k} \right) r_{(i,k)} \sigma_i \sigma_k \tag{10}$$

It should be noted that μ_y's in 9 are approximated to nominal values, which are presented in Figures 4(a) and 8(a). In addition, the read SNM and CWLM show linear dependences to the variations in the random variables (x_i) [37, 38]. Thus, the derivatives in 10, $\partial f/\partial x_i$, were easily found by using the metric values through the simulations at some values of x_i near the nominal values (η_i). Here, we used the cell sigma concept as the yield figure of merit of the SRAM. It is defined as the minimum amount of variation needed to cause a read or write failure. The cell sigma is given by the mean (μ) divided by the standard deviation (σ) [11]. Nowadays, six-sigma (6σ) yield or larger is required for large SRAM arrays [11].

We have plotted the read SNM cell sigma for all the cell structures in Figure 9. The read SNM cell sigma of the SAXP is the highest among those of all other structures at $V_{dd} \geq 0.8$ V. For $V_{dd} < 0.7$ V, the read SNM cell sigma of the AXP structure becomes the highest. For the AXN cell, in the cases of symmetric and asymmetric stress, the yield goes slightly below six at $V_{dd} = 0.5$ V. For all other cells, the read cell sigma yields are always larger than six. The non-monotonic behaviors observed for the structures may be explained using a similar reasoning to the one used for Figure 4.

Next we study the effect of process variation on the write margin. The write margin cell sigma values of different structures for without stress and after asymmetric stress in the worst case (second write) is plotted in Figure 8(b). For this parameter, for all V_{dd}'s, the AXN structure has the highest sigma. For the supply voltages of 0.6 and 0.5 V, the next highest write margin cell sigma belongs to the SAXP. The high cell sigma at low V_{dd}'s for this structure is attributed to the about constant nominal write margin (see Figure 8(a)) and lower sensitivity to the parameter variations at these voltages. Notice that only the SAXP structure has read and write sigma yields larger than six at $V_{dd} = 0.5$ V while the read yield of AXN and write yields of SAXN and AXP are below six for this supply voltage. In these structures, some work function tunings may be used to improve the yields. For example, using 4.67 eV, 4.63 eV, and 4.68 eV for AXN, SAXN, and AXP, respectively, provides equal read and write sigma yields of about 7.1, 6.4, and 7.3, respectively at $V_{dd} = 0.5$ V. The read and write cell sigma yields for the SAXP at this V_{dd} is 7.6 which is still the largest.

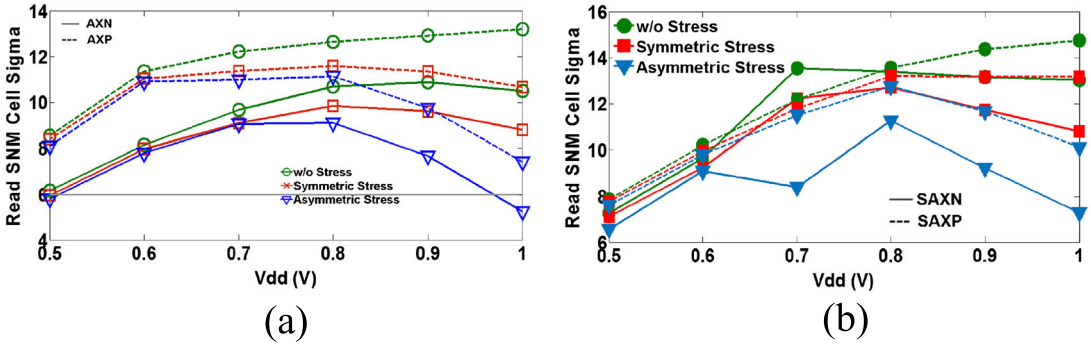

Figure 9. Read SNM cell sigma versus the supply voltage for (a) unstrained and (b) strained AXN (line) and AXP (dotted) structures. The stress time was assumed to be 1×10^8 s.

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Table II. Summary of important parameters of the cells.

	Read SNM degradation (symmetric stress) @V_{dd} = 1 V after 3 years	Read SNM degradation (asymmetric stress) @V_{dd} = 1 V after 3 years	Cell sigma yield with workfunction tuning @V_{dd} = 0.5 V	Size
AXN	12%	50%	7.1	497 nm × 220 nm
SAXN	11%	44%	6.4	497 nm × 220 nm
AXP	14%	43%	7.3	497 nm × 220 nm
SAXP	6%	33%	7.6	497 nm × 220 nm

5.3. Pros and cons comparison of the cells

In this subsection, we compare the pros and cons of the structures. Compared to the case of unstrained pMOS transistors, the read SNM of the proposed structure SAXP was lower. When used with two fins pull-up, SAXP had a read SNM larger than that of the AXP. Additionally, the write margin of SAXP was higher compared to that of AXP. In addition, the two fin SAXP cell had the highest read current with the lowest degradation due to the aging compared to the other structures. The two fin SAXP had a moderate write stability which was not degraded with the supply voltage scaling while the write stabilities of the other structures were noticeably degraded with the scaling. Although the write stability decreases by using two fins, its amount was sufficient for providing cell sigma value larger than six (see Figure 8(b)). Using two fins for the other structures would considerably deteriorate their write stabilities at low supply voltages, and hence, might not be invoked. In terms of the area, all the cells would be the same if the spacer pattern technology were used.

On the other hand, compared to the case of the unstrained pMOS transistors, the use of the strained transistors increased the read SNM of the conventional AXN cell while decreasing its write margin. The write margins for SAXN decreased faster with lowering V_{dd} yielding the lowest write margin among the structures at V_{dd} = 0.5 V. Finally, the static powers of all the structures (including the proposed SAXP with two fins pull-up) for all the supply voltages were below 10 nW per cell (due to using a near midgap gate workfunction).

The process variation study also showed that the proposed cell had the read and write cell sigma values higher than six for the supply voltages down to 0.5 V. However, the read or write cell sigma values of the other structures decreased to less than six at the lower end of the supply voltage range. Through some work function tuning, the cell sigma parameters of these structures also became larger than six but still less than those of the proposed structure. In summary, the SAXP structure which had robustness against BTI at high supply voltages and high yield at low supply voltages may be considered a better cell structure. A summary of important parameters of the cells is given in Table II.

6. CONCLUSION

In this work, we proposed a SRAM cell structure based on pMOS access transistors and predischarged bitlines. To limit the impact of NBTI/PBTI aging phenomena on the read SNM at high supply voltages, we used strained pMOS transistor technology. To have comparable read SNM, the fin number of pull-up transistors increased to two in the structure. In addition to a partial compensation of the NBTI effect due to invoking strain, in the case of symmetric stress, the PBTI effect was compensated by the NBTI effect. The efficacy of the proposed SRAM cell was studied using mixed mode device/circuit simulations for a gate length of 22 nm. The results showed that the read SNM degradation due to the symmetric aging at the supply voltage of 1 V was about 6% after three years for the strained proposed structure (SAXP), while they were 14%, 12%, and 11% for unstrained proposed structure (AXP), unstrained (AXN), and strained (SAXN) conventional structures, respectively. In addition, the SAXP cell had the highest read current compared to those of the other structures. The degradation of this current due to the aging was the lowest. In addition, the static powers of all the structures at all the supply voltages (including the strained proposed structure with two fins pull-up)

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were below 10 nW per cell (due to using near midgap gate workfunction). In addition, the write margin which degrades at low V_{dd}'s for conventional structure was relatively supply voltage independent for our proposed structure with strained pMOS. The study of the cell parameters in the presence of the process variation also showed that the proposed cell had the read and write cell sigma yields higher than six for different supply voltages ranging from 1 V down to 0.5 V. The read or write yields of the other structures, however, decreased to less than six in the lower end of the supply voltage range. Through some work function tuning, the cell sigma yields of these structures also became larger than six but still less than those of the proposed structure.

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