Dynamic Driver Supply Voltage Scaling for Organic Light Emitting Diode Displays

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***Abstract*—Organic light emitting diode (OLED) display is a self-illuminating device that is supposed to be power efficient than liquid crystal display (LCD). However, OLED display panels consume as much power as LCD panels due to total internal refection. As the power consumption of the OLED panel depends on the pixel colors, most previous power saving methods alter the pixel colors. In practice, such OLED power saving techniques can hardly accommodate photo viewers and movie players.**

This paper introduces the first OLED power saving technique that dynamically changes the supply voltage of the panel. Reduced supply voltage results in both power saving and decreased pixel luminance, but model-based color correction restores the decreased luminance with minimum color distortion. This technique is similar to dynamic backlight scaling of LCDs but is based on the unique characteristics of the OLED drivers. We provide an online color compensation algorithm using the luminance histogram. Luminance quantization in the histogram also achieves resource minimization. We develop a prototype and demonstrate the proposed OLED dynamic voltage scaling (DVS). Experimental result shows that the proposed OLED DVS saves up to 74.7% of the display power for the still images and up to 35.9% for movie clips.

I. Introduction

DISPLAY systems are primary sources of power consumption in battery-powered electronics despite the advances in low-power display technologies. As of today, liquid crystal display (LCD) panels are widely used in portable as well as desktop systems. The LCD panels do not illuminate themselves and require a high intensity backlight, which generally consumes a significant amount of power due to low transmittance of the LCD panels [2], [3]. On the other hand, an organic light emitting diode (OLED) is self-illuminating using organic light emission material. Therefore, OLEDs should provide higher brightness, higher luminance, faster response, wider viewing angle, and thinner and lighter-weight form factors compared with conventional LCD panels [4]. One of the known major disadvantages of OLED panels was their relatively short lifetime, which has been enhanced to be commercialized. However, the power efficiency of the OLED panels is not as high as expected due to serious total internal refection. As a result, most OLED smartphone users do not really feel extended battery life from the OLED display.

There have been extensive efforts to reduce the OLED panel power consumption. Most previous work attempted aggressive dimming of a part of the panel to reduce power consumption because the OLED power consumption is directly dependent on the pixel color. As red, green, and blue colors show distinctly different power efficiency, color swapping was also proposed. We summarize the previous work in Section II.

In this paper, we introduce OLED dynamic voltage scaling (DVS). We dynamically change the supply (driving) voltage of the OLED panel and save power. The proposed technique exploits the unique characteristics of the OLED driver circuits. The supply voltage of an OLED driver circuit is set to high enough voltage to support the full luminance of a pixel. An excessive voltage is generally supplied to the most pixels for most of the time, which gives headroom to apply supply voltage scaling. However, we cannot avoid minor pixel distortion because all the pixels have one power supply source, and pixel-level DVS is not allowed. Reduced supply voltage alters the pixel color value even with non-negative headroom. We restore the original pixel color by the use of model-based color compensation method.

We summarize major technical contributions of this paper as follows:

- Development of the concept of DVS for the OLED displays.
- Power analysis and modeling of OLED display.
- Development of the OLED DVS model.
- Image compensation algorithm that minimizes pixel color distortion after DVS.
- Online method based on the luminance histogram and histogram optimization by luminance quantization.
- Prototype implementation.

The rest of the paper is organized as follows. Section II summarizes previous research on low-power techniques for the display system. Section III introduces characteristics of the OLED cell, driver circuits and the principles of operation of the OLED DVS. Section IV presents a power optimization algorithm while maintaining the image distortion within a given threshold. Section V presents an online OLED DVS method based on the luminance histogram and its optimiza-

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TABLE I
CLASSIFICATION OF DISPLAY POWER SAVING TECHNIQUES.

Techniques	Features	Applications	Displays
Usage behavior monitoring	Not functional during low-power mode	Interactive applications	CRT, LCD and OLED
Partial display turn off	Disable objects not in interest	Mixed active /idle objects	LCD* and OLED
Color remapping	Altered look and feel	GUI	LCD and OLED
Backlight scaling	Minor color distortion	No restrictions	LCD

*LCD panels with zoned backlighting.

tion. Section VI introduces the prototype implementation, and Sections VII presents the experimental results.

II. RELATED WORK

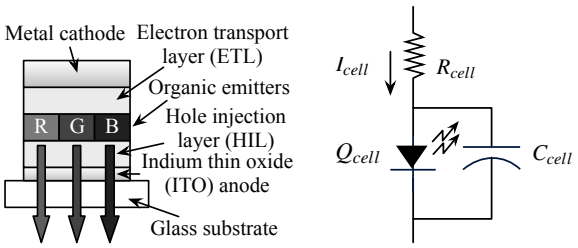
One of the simplest display power saving methods is brightness dimming or timeout-based display turnoff, which is actually widely used for most commercial products. Such a method can save display power at the direct expense of inconvenience. On the other hand, intensive research has been made to minimize user inconvenience as summarized in Table I. The first two categories of techniques disable the display functionality of the entire panel or part of the panel whereas the last two categories of techniques apply a transformation to the image being displayed.

Most high-level power saving methods are based on *idleness* of the system. Display does not generally have idleness while it is turned on. Nevertheless, first category methods actively detect idleness of the display detecting human eye gaze by the use of a camera [5], [6]. These techniques are applicable to any types of display with an interactive application where the user does not always pay attention to the display.

The second category of techniques is dedicated to LCD with zoned backlighting and OLED displays that allow partial display turnoff [7], [8]. This method is useful for distinguishable foreground and background objects such as multiple windows operating systems. Only active foreground objects have the original backlight luminance and other background or inactive objects have backlight turned off or dimmed [7]. OLED panel can freely change the colors of objects that are out of focus to dark colors [8].

The third category of techniques is also dedicated to LCD and OLED displays. They attempt content (color) change of the displayed image exploiting the power consumption difference by the pixel colors [9], [10], [11]. LCD panels exhibit around 10% power consumption difference due to change in the colors being displayed [12]. In addition, pixel color remapping provides more headroom for backlight dimming and, in turn, higher power saving [9]. Color remapping also has a big impact on the OLED panel power consumption [10]. Unfortunately, color remapping is not always feasible. It is applicable only to the graphics user interface (GUI) and applications not dealing with natural images, photos, or video.

Techniques in the last category reduce the backlight luminance and adjust colors to enhance the brightness and/or contrast of the image to compensate the image quality degradation [2], [3], [13], [14], and [15]. These backlight scaling techniques do not incur noticeable image degradation, nor does it result in a large color change. The LCD backlight scaling is widely used for commercial products nowadays.



(a) OLED device structure (b) Equivalent circuit model

Fig. 1. Device structure of OLED (a) and equivalent circuit model (b).

Unfortunately, backlight scaling cannot be applicable to self-illuminating display devices such as the OLED panels. Recent work introduces supply voltage scaling of the OLED derivers [1]. This method i) induces only minimal color change to accommodate display of natural images and ii) is applicable to only the displayed object that is of interest to the users. As the power consumption of an OLED panel is dependent on each pixel color value, existing OLED power management techniques are not capable of altering power consumption of the OLED panel while keeping the pixel color values. Follow-up research introduces a DVS-friendly OLED driver circuit design [16]. It maintains the cell current when the supply voltage scales by adding additional transistor on the gate side of the driver transistor. This paper is an extension of the basic OLED DVS presented in [1].

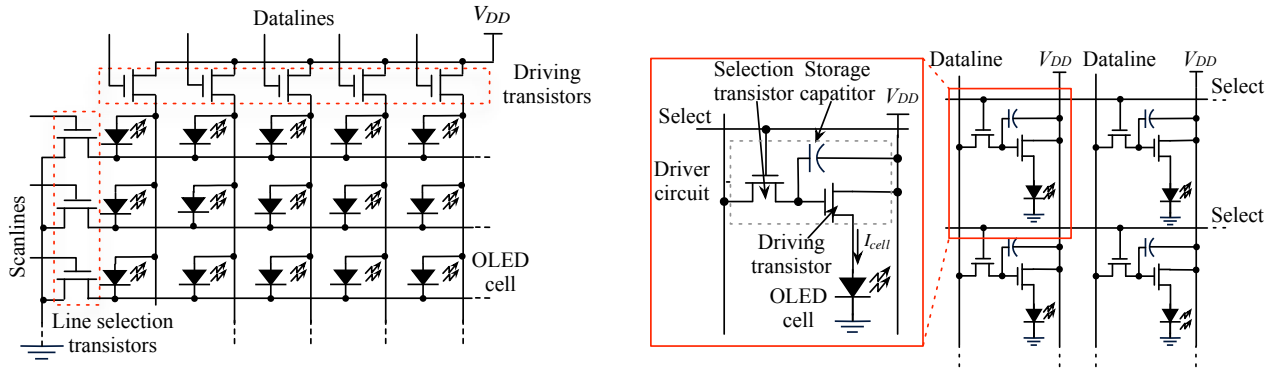
III. SUPPLY VOLTAGE SCALING OF OLED DRIVERS

A. OLED display structures and driver circuits

Fig. 1(a) shows the typical structure of the OLED cell [4]. The OLED device has a large area, but the thickness of the organic layers between the electrodes is only 100–200 nm. As a result, OLED cells have a large internal capacitance. The value of C_{cell} is typically 200–400 pF/mm^2. OLED cells have a resistive component for each layer that lies between anode and cathode. An Indium-Thin-Oxide (ITO) layer is the dominant resistive component. Hence, the parasitic resistor is in series with the internal capacitance. The value of the parasitic resistor is strongly dependent on the design of the ITO electrode (anode). A typical value of the cell resistance is 15Ω/sq[1]. We calculate the R_{cell} with the cell area and sheet resistance. A simple equivalent circuit obtained with the physical parameters is depicted in Fig. 1(b). It consists of the parasitic resistor R_{cell}, internal capacitance C_{cell}, and a diode Q_{cell}.

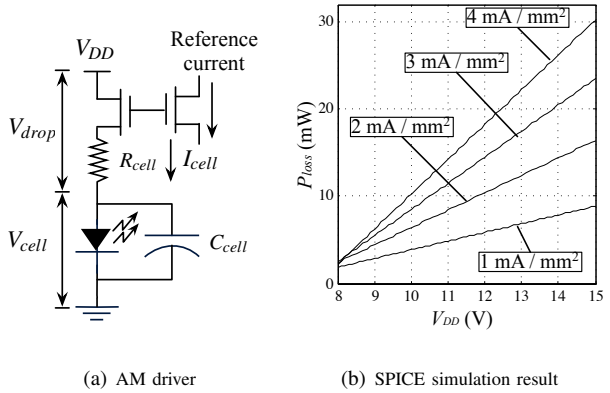
There are several ways to classify the OLED driver architectures. Like LCD panels, an OLED panel may have either a passive matrix (PMOLED) or an active matrix (AMOLED) structures. A PMOLED panel has simpler structure and thus lowers cost. However, the practical maximum size is limited, typically up to 3". PMOLED panels have a row-column

[1]Ω/sq denotes the sheet resistance.



(a) Passive-matrix OLED display (b) Active-matrix OLED display

Fig. 2. Panel structures of OLED displays: (b) active-matrix OLED display and (a) passive-matrix OLED display.



(a) AM driver (b) SPICE simulation result

Fig. 3. Behavioral concept of (a) AM driver and (b) SPICE simulation result of P_{loss} with different V_{DD} and I_{cell} in AM driver circuit.

structure driver circuit as shown in Fig. 2(a). There is no storage capacitor in the PMOLED driver circuit. The cell current can be a pulsed current. In contrast, a thin film transistor (TFT) with a storage capacitor controls every pixel of AMOLED panels similar to the TFT LCD panel as shown in Fig. 2(b). AMOLED panels can accommodate large size and high fidelity display.

The OLED cell current, I_{cell}, determines the luminance. The cell current is basically controllable by adjusting the cell voltage, V_{cell}. However, we commonly use a constant current driver because the parasitic resistance is not stable. A current mirror current steering circuit forms an amplitude modulation (AM) driver. The AM driver scheme ensures a higher reliability and efficiency of the OLED cells. The current steering circuit consumes large area, which results in higher cost.

An alternative way of current control is a pulse width modulation (PWM) of the cell current, which is common in the PMOLED panels. The luminance of an OLED cell is dependent on the average value of I_{cell}. The PWM cell current steering circuit is inexpensive and provides precise luminance control. However, it is known to be less power efficient in high luminance region [4].

B. V_{DD} scaling for AM drivers

The concept of DVS of an OLED panel is to reduce power loss due to V_{drop} by scaling down V_{DD}. Although we scale down the V_{DD} of the AM driver circuit, there is only small change in I_{cell} due to the Early Effect in the AM driver as far as the driving transistor remains in the saturation mode (Fig. 3(a)). The driving transistor enters the triode mode when I_{cell} becomes too large with the scaled V_{DD}. The cell luminance decreases as we scale down V_{DD} in the triode mode, which causes image distortion.

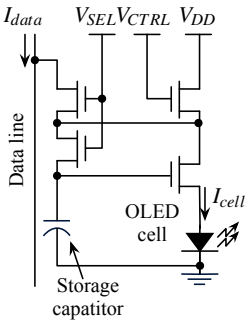


Fig. 4. DVS-friendly AM driver circuit [16].

The power loss of OLED cell is defined by $P_{loss} = I_{cell}V_{drop}$ where V_{drop} is determined by the characteristics of the OLED cell and I_{cell} is determined by the saturation current of the driver transistor. The V_{DD} should be dropped by power dissipation in the driver transistor, and P_{loss} due to $V_{drop}$is given by

$$P_{loss} = I_{cell}V_{drop} = I_{cell}(V_{DD} - V_f), \quad (1)$$

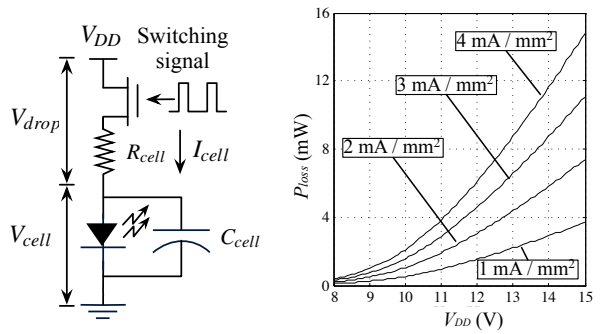
where V_f is the forward bias voltage of the diode.

Fig. 3(b) shows a SPICE simulation to estimate P_{loss} with the parameters from [4]. The simulation model has V-I characteristics as follows:

$$I_{cell} = 1.4144 \cdot 10^{-6}(e^{\frac{V_{cell}}{0.93678}} - 1),$$

with 20 mm^2 active area. We estimate P_{loss} with various V_{DD} values while delivering four different I_{cell} values from 1 mA/mm^2 to 4 mA/mm^2. The simulation result depicted in Fig. 3 (b) shows that $P_{loss}$is proportional to the V_{DD} and I_{cell} as described in (1).

Fig 4 depicts a DVS-friendly OLED driver circuit that is more amenable to supply voltage scaling [16]. The DVS-friendly driver makes color distortion happen only when V_{DD} is too low to supply I_{cell} = I_{data} because the bias condition



(a) PWM driver (b) SPICE simulation result

Fig. 5. Behavioral concept of (a) PWM driver and (b) SPICE simulation result of P_{loss} with various V_{DD} and I_{cell} values.

of T_4 is maintained by storage capacitor and V_{ctrl}. So, I_{cell} is equal to I_{data} as long as the V_{DD} is high enough. The DVS-friendly AM driver makes OLED DVS more efficient.

C. V_{DD} scaling for PWM drivers

DVS acts a bit differently in a PWM driver (Fig. 5 (a)). Scaling V_{DD} down directly affects I_{cell}. We have to restore the luminance of image even with a slight V_{DD} scale. We apply model-based image compensation and restore the luminance. A brighter color makes a higher PWM duty ratio in the PWM driver. The image compensation cannot always restore the original luminance if the original I_{cell} is too large. The maximum possible I_{cell} under the scaled V_{DD} cannot be the same as the original I_{cell} even when the PWM duty ratio is set to 100%. Thus, luminance distortion for some very bright pixels becomes unavoidable. We sacrifice a small display quality by allowing a certain amount of color distortion of the image but save significant amount of power consumption.

With the PWM drivers, V_f and R_{cell} determine the maximum value of I_{cell} as follows:

$$I_{cell} = \frac{V_{DD} - V_f}{R_{cell}}. \tag{2}$$

The luminance of the OLED is approximately proportional to the average value of I_{cell}, $\overline{I_{cell}}$, which is calculated by

$$\overline{I_{cell}} = I_{cell} d = I_{cell} \frac{t_{on}}{t_{on} + t_{off}}, \tag{3}$$

where PWM duty, $d = t_{on}/(t_{on}+t_{off})$, and t_{on} and t_{off} are the switch turn on and off durations in a PWM period, respectively. The power loss of an OLED cell during a PWM period is given by

$$P_{loss} = \overline{I_{cell}}^2 R_{cell}. \tag{4}$$

Fig. 5 (b) shows a SPICE simulation result to estimate P_{loss} of the PWM driver such that P_{loss} quadratically increases as the V_{DD} and I_{cell} increase as described in (4). We use the same simulation parameters in Section III-B. We estimate P_{loss} with various V_{DD} while delivering four different I_{cell} values from 1 mA/mm^2 to 4 mA/mm^2.

IV. Power optimization considering image quality

A. Image quality and power models of OLED panels

We use human perception-aware color model to evaluate the image distortion. Typical RGB and CMYK spaces reflect the output of physical devices rather than human visual perception. CIE Lab color space is designed to approximate human-perceived vision. It is derived from the CIE 1931 XYZ color space, which reflects the spectral distribution of colors, and can be computed via simple formulas from the XYZ space. Due to its perceptual uniformity, its L component closely matches the human perception of brightness. The Euclidean distance in the Lab color space is widely used as a metric to measure the human perceived color difference [17].

The XYZ measurement result shows that X, Y, and Z values of RGB pixels are highly correlated (almost linearly proportional) with the cell current or almost constant regardless of the cell current. We build a transformation function using regression analysis, which is given by

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} I_{cell} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix}, \tag{5}$$

where coefficients a_X, a_Y, a_Z, b_X, b_Y, and b_Z are obtained by performing the regression analysis on the measurement results.

We construct an I_{cell} model for a PMOLED panel with a PWM driver based on (2) and (3). The cell current I_{cell} is proportional to V_{DD} and d such that

$$I_{cell}(d, V_{DD}) = p_1 V_{DD} d + p_2 d + p_3, \tag{6}$$

wherep_1, p_2, and p_3 are characteristic coefficients.

We describe the human-perceived image difference with the Euclidean distance in the CIE Lab color space. We transform $I_{xyz} = (X, Y, Z)$ into a Lab color space image such that $I_{lab} = (L, a, b)$ by using the following transform functions [18].

$$\begin{aligned} L &= 116 \cdot (Y/Y_w)^{\frac{1}{3}} - 16 \\ a &= 500 \cdot ((X/X_w)^{\frac{1}{3}} - (Y/Y_w)^{\frac{1}{3}}) \\ b &= 200 \cdot ((Y/Y_w)^{\frac{1}{3}} - (Z/Z_w)^{\frac{1}{3}}), \end{aligned} \tag{7}$$

where L, a and b are matrices representing brightness, red-green content, and yellow-blue content in the Lab color space, respectively. Values of X_w, Y_w, and Z_w are the color coordinate values of the reference white in the color space. The Euclidean distance between two different colors $c_1 = (L_1, a_1, b_1)$, $c_2 = (L_2, a_2, b_2)$ in the Lab color space is calculated by

$$\varepsilon = \sqrt{(L_1 - L_2)^2 + (a_1 - a_2)^2 + (b_1 - b_2)^2}. \tag{8}$$

B. OLED display characterization

We chose a target OLED panel from Univision Technology [19], UG-2076GDEAF02, that has a 2.2" display area, a 220×176 resolution and a PMOLED structure with a PWM driver. We measure the relationship between the power consumption and luminance/chromaticity of the OLED panel with various V_{DD} values and pixel colors. We setup the measurement environment as shown in Fig. 6. We control V_{DD} with a

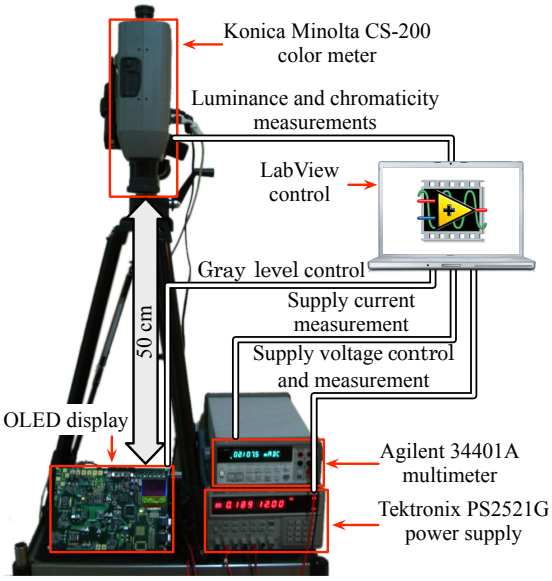


Fig. 6. Experimental setup for the OLED display panel characterization.

programmable power supply and measure the current with an Agilent 24401A digital multimeter. We use a Konica Minolta CS-200 color meter to measure the luminance and chromaticity of the OLED panel. The experiment is automated by using a National Instruments LabView console. We perform the entire measurement process in a darkroom to block the effect of ambient light. We acquire the coefficients by measurement and summarize them in Table II. They show that the OLED cell of the UG-2076 OLED display panel has approximately 15 Ω of R_{cell} and 7.4 V of V_f.

We visualize a part of characterization data in Fig. 7. The OLED display achieves the same luminance by adjusting the color value (gray level here) even with different V_{DD} levels. In other words, we can restore the color value with even a reduced V_{DD}, which proves the key premise of DVS for OLEDs. Fig. 7 shows that the OLED panel generates a 70 cd/mm^2 luminance with a 15 V, a 13 V, a 11 V, and a 9 V V_{DD} by setting the gray level to 57%, 59%, 64%, and 77%, respectively. It turns out that the luminance is not affected by V_{DD} when the gray level is below a certain level such as non-linear region in Fig. 7. Therefore, we compensate the V_{DD} scaling-induced luminance reduction by modifying image data only in the linear region of Fig. 7.

TABLE II
EXTRACTED PARAMETERS FOR THE POWER ESTIMATION AND IMAGE DIFFERENCE EVALUATION (I_{cell} IS IN μA).

		R		G		B
I_{cell} estimation	p_1	2.222e-2	p_1	2.234e-2	p_1	2.245e-2
	p_2	-1.650e-1	p_2	-1.648e-1	p_2	-1.599e-1
	p_3	1.652e	p_3	1.664e0	p_3	1.597e0
Image difference evaluation	a_X	3.573e5	a_X	1.035e5	a_X	4.903e4
	b_X	-4.554e-1	b_X	-2.764e-1	b_X	-3.230e-1
	a_Y	1.793e5	a_Y	2.556e5	a_Y	6.139e4
	b_Y	-2.282e-1	b_Y	-7.086e-1	b_Y	-3.020e-1
	a_Z	0.000e0	a_Z	2.263e4	a_Z	2.384e5
	b_Z	7.100e-3	b_Z	-6.030e-2	b_Z	-1.937e1

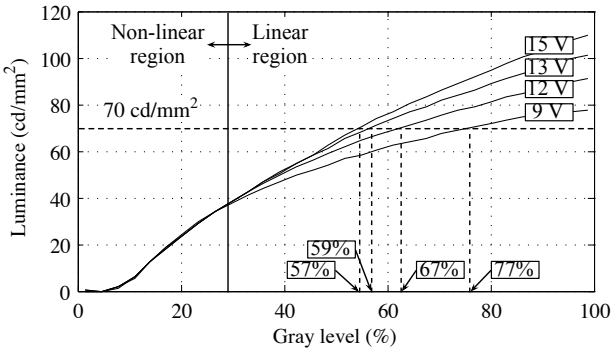


Fig. 7. Measured luminance by V_{DD} and gray level with AM driver.

C. V_{DD} scaling and image compensation

The transistor in the AM driver is originally designed to operate in the saturation mode. The driver transistor is in the saturation mode though we scale V_{DD} as shown in Fig. 8 as long as V_{DS} is higher than $V_{GS}-V_T$. The saturation mode operation ensures the almost same I_{cell} regardless of changes in the V_{DD}. There is only small change of I_{cell} due to the Early effect. Consequently, V_{DD} scaling only affects pixels with high brightness as shown in Fig. 8. High brightness pixels can no longer deliver the same amount of the cell current with a reduced V_{DD}. We need to limit the number of distorted pixels to maintain the image quality, and V_{DD} should be determined under the considerations of the upper bound of the distorted pixels.

We have more potential to save power consumption from V_{DD} scaling with the PWM drivers. We reduce P_{loss} in an OLED cell while preserving the luminance in spite of a reduced V_{DD} by raising d according to (2), (3), and (4). The scaled V_{DD} for PWM drivers evenly decreases the luminance of all the OLED cells. At the same time, we restore $\overline{I_{cell}}$ and the luminance by increasing the PWM duty ratio d in (3) as shown in Fig. 9. Then we obtain the same $\overline{I_{cell}}$ with less P_{loss}.

The CIE Lab color space regards two different colors perceptually identical when the Euclidean difference between the two color points is less than a certain threshold. The threshold is generally determined by the human vision characteristics and environmental conditions, and the user also can determine it. We formulate an optimization problem

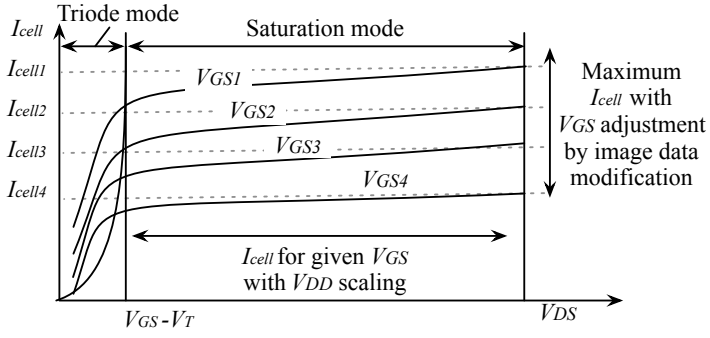
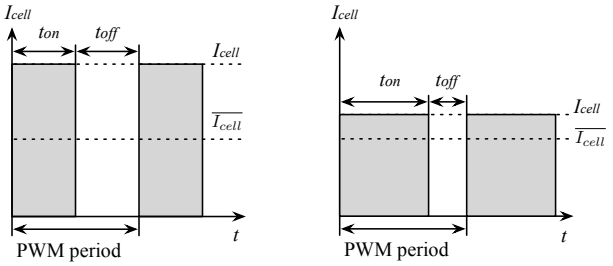


Fig. 8. Effect of V_{DD} scaling and image compensation on the OLED cell current with AM drivers.



(a) OLED cell current with the maximum V_{DD} (b) OLED cell current with the scaled V_{DD}

Fig. 9. Effect of V_{DD} scaling and image data modification on OLED cell current with (a) the maximum V_{DD} and (b) scaled V_{DD} for PWM drivers.

to find a transformed image $I' = (R', G', B')$ and V_{DD} that maximize the power saving subject to the given threshold for indiscernible colors. The threshold, τ_{image}, can be thought of as the maximum allowable average Euclidean distance $\bar{\varepsilon}$ between the original and compensated images. We develop an iterative algorithm to find the solution with image quality and power model of the OLED display as shown in Algorithm1.

Fig. 10 illustrates the behavior of the OLED DVS algorithm with the OLED panel. Upper surface plot of Fig. 10 shows the OLED panel power consumption and lower surface plot shows the luminance value according to the gray level of pixels and V_{DD}. The 'Original' dot in the Fig. 10 represents the original V_{DD} and gray level. The dot moves straight down by V_{DD} scaling ((a) in Fig. 10), losing luminance and consuming less power. The image compensation ((b) in Fig. 10) recovers the luminance with a higher gray-level value. This new gray-level incurs higher power consumption, but the 'Scaled' dot eventually exhibits lower power consumption than that of the 'Original' dot while having the same luminance. As the available voltage levels are limited desecrate values, V_{DD} and gray level are discrete, too. Algorithm 1 depicts how to iteratively derive the optimal discrete V_{DD} and gray scale level.

Algorithm 1: Algorithm for OLED DVS.

Input: Image $I = (R, G, B)$ and image distortion tolerance τ_{image}.

Output: Transformed image I'

1: Set V_{DD} at the maximum supply voltage V_{max}.
2: Decrease a V_{DD} step ΔV_{DD} from the previous V_{DD}.
3: Calculate the power reduction by (6).
4: Calculate the average image distortion $\bar{\varepsilon}$ caused by V_{DD} scaling by (8).
5: Calculate minimum grayscale step increment for R, G, and B by (6)–(8) to increase enough amount of I_{cell} to satisfy the image distortion tolerance constraint ($\bar{\varepsilon} \leq \tau_{image}$).
6: Calculate the power of the modified image and scaled voltage by (6).
7: If the voltage scaling induced power reduction is less or equal to the required power to satisfy the the image distortion tolerance constraint, then stop the DVS.
8: Otherwise, repeat 2–7.

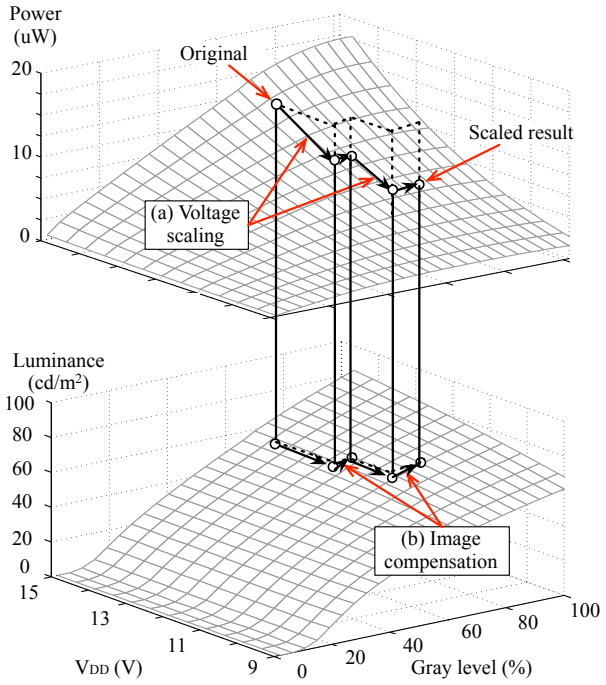


Fig. 10. Power and luminance measurement with a different V_{DD} and image data.

The major computational overhead of OLED DVS is the estimation of the image distortion and calculation of image compensation. We derive them by using a pre-generated lookup table depending on the characteristics of the OLED panel and the driver architecture [2]. The number of color values and V_{DD} levels determine the table size. These parameters strongly affect the performance obtained by the proposed OLED DVS scheme such as delay penalty to display/update an image on the OLED panel and power saving. We introduce a design optimization of the OLED DVS system considering power, image quality, and required resources in Section V.

V. Hardware Support for Online OLED DVS

We design hardware support unit for an online OLED DVS control. We use pixel luminance histogram and build a lookup table with the scaled V_{DD} as the input and estimates of the image distortion as the output. The estimation identifies pixels having higher luminance value that cannot be produced with the scaled V_{DD} even after image compensation.

We count the number of pixels from the brightest one to limit the image distortion within τ_{image}. More precise characterization result is obtained with smaller intervals in the histogram [3]. We estimate the side effect in power saving from the histogram quantization interval and derive the most efficient quantization granularity.

A. Estimation of image distortion

Fig. 11 shows how to derive the threshold luminance L_T as a function of d and V_{DD} from (5), (6), and (7). The luminance

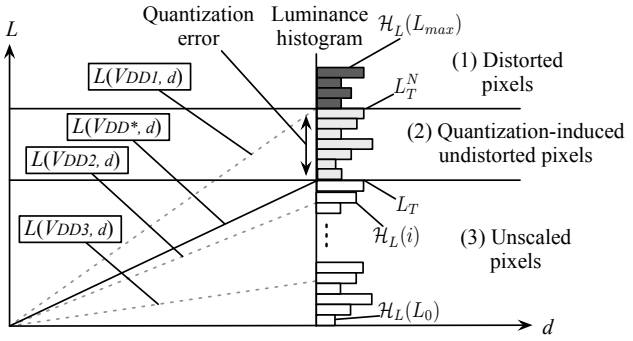


Fig. 11. Side effect in power saving due to the quantization in the histogram.

threshold L_T represents an upper limit of luminance that is not distorted by the V_{DD} scaling. The highest possible luminance value without V_{DD} scaling is L_{max}. We define L_T corresponding to the image distortion threshold τ_{image} by the following condition:

$$\sum_{i=L_T}^{L_{max}} D(i)\mathcal{H}_L(i) \le \tau_{image} \text{ and } \sum_{i=L_T-1}^{L_{max}} D(i)\mathcal{H}_L(i) > \tau_{image}, \quad (9)$$

where $\mathcal{H}_L(i)$ represent the number of pixels whose luminance value is i, and $D(i)$ represents the corresponding distortion value. Pixels with the luminance higher than L_T (Fig. 11 (1) and (2)) will be distorted even with a histogram without quantization. OLED DVS reduces P_{loss} by scaling V_{DD} to V_{DD}^* corresponding L_T where V_{DD}^* denotes required voltage level to illuminate the pixels at L_T with the maximum d value. Pixels with the luminance lower than L_T (Fig. 11 (3)) are restored by the image compensation.

Histogram quantization in image compensation [3] affects the upper limit of luminance that is not distorted by the V_{DD} scaling. Let us denote the luminance value with a quantized N-step histogram as L_T^N. Quantization error makes $L_T \le L_T^N$.

$$L_T^N = \lceil \frac{L_T}{(L_{max}/n)} \rceil \frac{L_{max}}{n}. \quad (10)$$

Pixels with the luminance higher than L_T^N (Fig. 11 (1)) are distorted because the luminance value should be mapped to L_T^N while pixels in (Fig. 11 (2)) are not distorted. However, less pixel distortion implies less power saving.

We analyze the amount of power saving sacrificed due to histogram quantization by the interval step, N. This is a guidance to obtain the optimal design of image analyzer considering accuracy and overhead. The difference between P_{loss} and ΔP_{loss} by V_{DD} and V'_{DD} is power saving, which is given by

$$\begin{aligned}&\Delta P_{loss}(V_{DD}, V'_{DD}, d) \quad (11)\\ &= R_{cell}\left[\left(\frac{V_{DD}-V_f}{R_{cell}}\right)^2 \cdot d - \left(\frac{V'_{DD}-V_f}{R_{cell}}\right)^2 \cdot d'\right],\\ &= R_{cell}\frac{V_{DD}-V_f}{R_{cell}} \cdot (V_{DD}-V'_{DD}) \cdot d\end{aligned}$$

where d' is determined by following equation to supply the same average I_{cell} with V_{DD} and V'_{DD}.

$$d' = \frac{V_{DD}-V_f}{V'_{DD}-V_f} \cdot d. \quad (12)$$

We calculate the difference of P_{loss} between the histogram with and without N-step quantization by V_{DD}^* and V_{DD}^{*N} that correspond to V_{DD} for L_T and L_T^N, respectively. We denote required voltage level to illuminate the pixels as L_T^N with the maximum d value by V_{DD}^*. Expectation of the difference between $\Delta P_{loss}(V_{DD}^*, V_{DD}^{*N}, d)$ is calculated by

$$\begin{aligned}&Exp(\Delta P_{loss}) = Exp(\Delta P_{loss}(V_{DD}^*, V_{DD}^{*N}, d)) = \quad (13)\\ &\sum_{j=L_0}^{L_{max}} \left\{ \sum_{k=L_0}^{\bar{j}} \sum_{l_k=0}^{N_{pixel}-N_{dist}} \left[\Delta P_{loss}(V_{DD}^*, V_{DD}^{*N}, d)) \cdot l_k \cdot Pr(l_k, j)\right] \right.\\ &\left. + \sum_{k=\bar{j}}^{L_{max}} \sum_{l_k=0}^{N_{dist}} \left[\Delta P_{loss}(V_{DD}^*, V_{DD}^{*N}, 1) \cdot l_k \cdot Pr(l_k, j)\right] \right\}.\end{aligned}$$

where $\bar{j}$ represents the corresponding L_T^N value for j, which is given by

$$\bar{j} = \lceil \frac{j}{(L_{max}/n)} \rceil \cdot \frac{L_{max}}{n}, \quad (14)$$

and the number of distorted pixel are calculated by

$$N_{dist} = \sum_{i=\bar{j}}^{L_{max}} \mathcal{H}_L(i). \quad (15)$$

We calculated d, V_{DD}^*, and V_{DD}^{*N} from (3), (5), (6) and (7). We denote the probability such that k-th interval in the histogram without quantization has l_k pixels where $L_T = j$ by $Pr(l_k, j)$, which is given by

$$\begin{aligned}&Pr(l_k, j) = Pr(\mathcal{H}_L(k) = l_k | L_T = j) \quad (16)\\ &= \left\{ \begin{pmatrix} N_{pixel} \\ N_T \end{pmatrix} (\frac{L_{max}-j}{L_{max}})^{N_T} (1 - \frac{L_{max}-j}{L_{max}})^{N_{pixel}-N_T} \cdot \right.\\ &\left. \begin{pmatrix} N_{pixel}-N_T \\ l_k \end{pmatrix} (\frac{1}{L_{max}})^{l_k} (1 - \frac{1}{L_{max}})^{N_{pixel}-N_T-l_k} \right\},\end{aligned}$$

where N_{pixel} is the total number of OLED cells on the panel, N_T is the number of pixels that have higher luminance than L_T, and the value of L is uniformly distributed from L_0 to L_{max}. Without loss of generality, each binomial probability mass function component in (16) can be approximated to the normal distribution because N_{pixel} is large enough and $N_{pixel} \cdot (1/L_{max})$ is far greater than 10 as far as N_T is smaller than 10 % of N_{pixel}.

We obtain the expected power saving with n-interval histogram by

$$\begin{aligned}Exp(P_{saving}) =& Exp(\Delta P_{loss}(max(V_{DD}), V_{DD}^*, d) \quad (17)\\ &- Exp(\Delta P_{loss}(V_{DD}^*, V_{DD}^{*N}, d),\end{aligned}$$

where the $max(V_{DD})$ is 15 V which is used in the implementation. Each histogram interval requires a counter register that can accommodate N_{pixel}. We consider the overhead of counters and calculate P_{saving} per counter, P_{saving}/n, to consider resource complexity. Fig. 12 shows $Exp(\Delta P_{loss})$ for different n

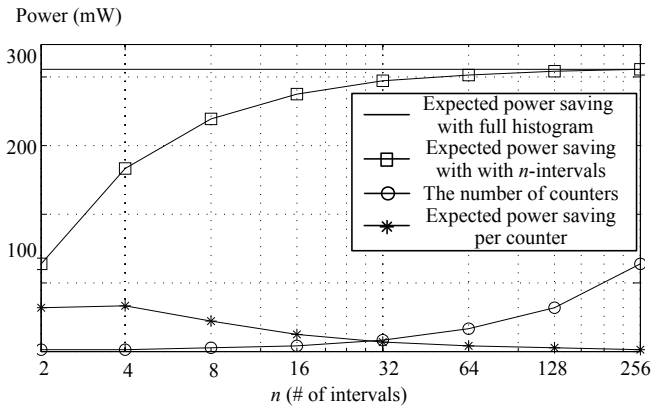


Fig. 12. P_{saving} vs. the number of counters.

in a 220 $\times$ 176 display panel with τ_{image} corresponding to the 5 % of totally distorted pixels. As shown in Fig. 12, P_{saving}/n decreases as $n > 4$. We confirm that 4-step histogram shows the most efficient results for the target OLED system.

B. V_{DD} transition overhead

Transition energy overhead in a DVS-enable system was carefully studied in [20]. When V_{DD} range is from 8 V to 15 V with a 22 μF output bulk capacitor in the DC-DC converter (which is used in our implementation), the required energy to charge the output bulk capacitor is about 0.76 mJ. The maximum voltage transition frequency is determined by the refresh rate of the OLED panel. If we use 60 Hz refresh rate, then the expected power overhead for the voltage transition is about 46 mW. However, as indicated in [20], the extra energy consumed as a result of scaling up V_{DD} can be compensated for by the V_{DD} downscaling. Consequently, the expected amount of wasted energy is negligible for random V_{DD} change.

Modern DC-DC converter requires for a few tens of μs for a voltage transition within the operating range [20]. OLED display panels have idle intervals during VSYNC period. The length of each VSYNC period is typically about 3 HSYNC cycles, and the HSYNC is asserted at the end of horizontal scan. Consequently, VSYNC period is about 9 horizontal scan cycles. The length of data transfer cycle is determined by the refresh rate and the display size. If we use 60 Hz refresh rate in 1920 x 1200 display, then the idle period between the refresh operation is about 130 μs. Therefore, the voltage transition is feasible during the idle period even when we use a large-size panel.

VI. Implementation

A. Hardware implementation

We develop an hardware board which enables V_{DD} scaling and the image compensation for the target OLED display panel. This platform equips two output voltage adjustable DC-DC converters for an UG-2076 OLED display panel. We modify the output voltage feedback loop of a LT3495 DC-DC converter form Linear Technology by using an AD5161 digital potentiometer from Analog Device. The platform is compatible with the peripheral interface of a Xilinx Virtex-5 FPGA-based evaluation platform. We control the OLED display panel and power converters through the FPGA platform. Supply voltage and current are measured by an INA194 current shunt monitor form Texas Instrument and an ADC102S Analog-Digital converter from National Semiconductor.

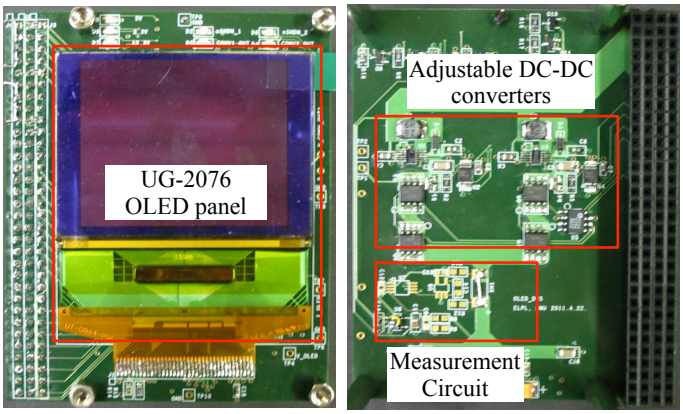


Fig. 13. Output voltage adjustable DC-DC converter equipped OLED display board.

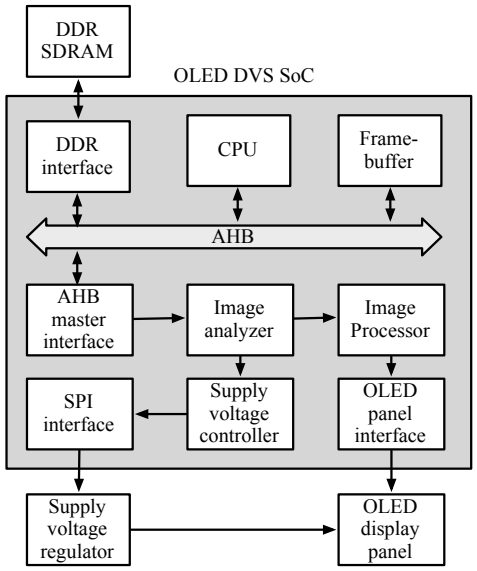


Fig. 14. OLED DVS enabled system-on-chip implemented with an FPGA.

B. OLED DVS System-on-Chip

We implement an OLED DVS system-on-chip (SoC) on a FPGA as shown in Fig. 14. The SoC consists of an ARM7 microprocessor, a DDR SDRAM interface, an on-chip SRAM framebuffer, an image analyzer, an image processor, a V_{DD} controller, and a SPI interface. The microprocessor transfers the image data to the framebuffer, and the AHB master interface provide the frame data to the OLED display panel interface according to the sweep rate of the OLED display panel. The image analyzer finds the optimal V_{DD} and a lookup table map of image data by constructing the histogram of the pixel data. According to the value obtained by the image analyzer, the V_{DD} controller adjusts the output voltage of

TABLE III
SYNTHESIS RESULT AND POWER MEASUREMENT OF OLED DVS UNIT IN FPGA.

		Original	OLED DVS
Synthesis result	Slices	8353	8993
	Slice Reg.	7910	8131
	LUTs	13261	14629
	LUTRAM	1109	1109
	BRAM	130	130
Power consumption		6.273 W	6.319 W

the V_{DD} regulator through the SPI interface, and the image processor modifies the pixel data synchronized with each other.

The image analyzer builds a luminance histogram of the image for each color. The image analyzer consists of pixel counter and registers storing threshold values. The number of counters accruing to the histogram steps in the image analyzer is synthesizable, and the threshold values are programmable by user. We separately setup the threshold values in the linear region and non-linear region according to the relation between the luminance and V_{DD} as shown in Fig. 7. We estimate the image distortion from the image histogram and select the V_{DD} level. The image processor consists of arithmetic operators and lookup table. The image data output value is calculated by a piece-wise linear model with the coefficients stored in the lookup table. The number of piece in the model is synthesizable, and the lookup table is programmable.

The OLED DVS unit accepts the V_{DD} level and original image data as an input, and generates a modified image data value to compensate the effect of V_{DD} scaling. The V_{DD} controller adjusts the output voltage of the DC-DC converter by changing the value of feedback resistance. We connect the digital potentiometer to the feedback input of the DC-DC converter. The resistance value of the digital potentiometer can be controlled by a serial peripheral interface (SPI). The V_{DD} controller transmits SPI signal synchronized with a frame synchronization signals.

Table III summarizes space complexity of the DVS-enabled OLED display panel controller synthesized in the FPGA. We measure the average power consumption of the Xilinx XUPV5-LX110T platform when the OLED DVS module is on and off with the same image sequence. The difference between the power consumption of OLED DVS enabled and disabled display controller is 46 mW that corresponds to 0.73% of the total power consumption. The synthesis result shows that the OLED DVS enabled system requires 7.66 % more slices (CLBs).

We also estimate the area and power overhead for an ASIC implementation. We obtain the silicon area and estimated power consumption value for the OLED DVS controller unit by using TSMC 45 nm technology with Synopsys Design Compiler. The results are summarized in Table IV.

TABLE IV
SILICON AREA AND ESTIMATED POWER CONSUMPTION OF OLED DVS UNIT WITH TSMC 45 NM TECHNOLOGY.

Area	
Number of nets	2274
Number of cells	173
Number of references	41
Combinational area	3667.179605
Noncombinational area	1181.527204
Total cell area	4848.706809
Power consumption	
Global operating voltage	0.99
Cell internal power	199.0935 uW
Net wwitching power	72.8849 uW
Total dynamic power	271.9784 uW
Cell leakage power	297.7593 uW

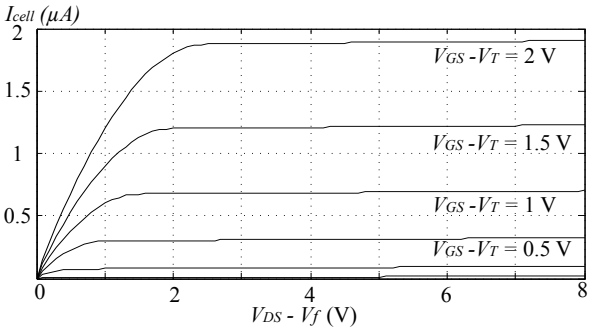


Fig. 15. TFT driver gate characteristics for simulation of OLED panel with AM driver.

VII. EXPERIMENTS

A. Simulation result for OLED display with AM driver

We implement a prototype by using an OLED display panel which equips PWM driver circuit. We perform a simulation to evaluate the effect of OLED DVS with AM driver-based OLED display. Fig. 15 shows the I-V characteristics of the driver gate. Based on the driver gate characteristics presented in Fig. 15 and optical characteristics presented in Section IV-B, we evaluate the OLED DVS with several standard test images. Fig. 16 shows the result for a Lena, a mandrill, a boat and an airplane. We use the characterization result presented in Section IV-B to calculate the power consumption and image distortion. The images in first row in Fig. 16 are original test images. The second row is V_{DD}-scaled images constrained by the number of distorted pixels. We limit the number of distorted pixels within 5%. The average power saving is 37%.

As described in Section IV-C we cannot compensate the image distortion with the AM driver circuit due to the current mirror operation in the saturated region. Therefore, the distortion of bright pixel is not avoidable. We show the location of distorted pixels in the last row of Fig. 16. The distorted pixels are represented by color inversion. We can see that the bright parts of the images are distorted.

We evaluate the histogram-based OLED DVS by simulation. Fig. 17 shows the V_{DD} scaling and estimated power result for the movie clip. We use 10 seconds of movie clip from the 'How to Train Your Dragon.' The movie clip is carefully chosen to contain bright scenes and dart scenes keeping the balance. V_{DD} is scaled up to 9 V while play the movie clip. The original movie clip with 15 V V_{DD} shows 5.45 J energy consumption during 10 s, and the movie clip with a 5% dis-

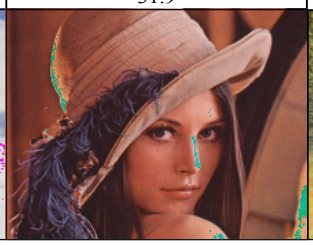
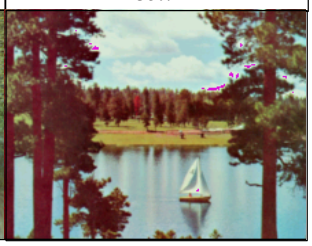
	Airplane	Lena	Mandrill	Boat
Original image				
V_{DD} (V)	15.0	15.0	15.0	15.0
Power (mW)	1412.9	367.7	665.8	734.4
Scaled image with 5 % distorted pixels				
V_{DD} (V)	9.32	9.49	9.55	9.64
Power (mW)	877.8	250.3	423.7	472.1
Saving (%)	44.1	31.9	36.3	35.7
Distorted pixels (inverted color)				

Fig. 16. Simulation results for AM driver-based OLED display with standard test images.

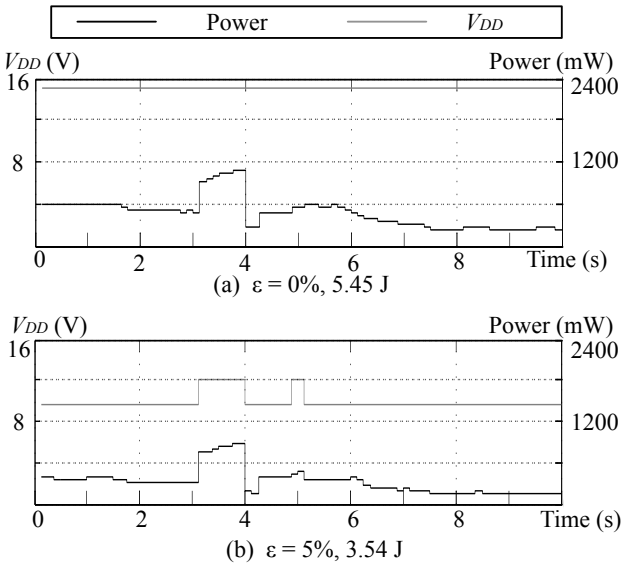


Fig. 17. Simulation results of power consumption with OLED DVS for the movie clips with (a) 0% distortion tolerance (b) 5% distortion tolerance.

tortion constraint shows 3.54 J.

B. Measurement result for OLED display with PWM driver

We evaluate the power gain and resultant image quality from the proposed OLED DVS on real still images and image

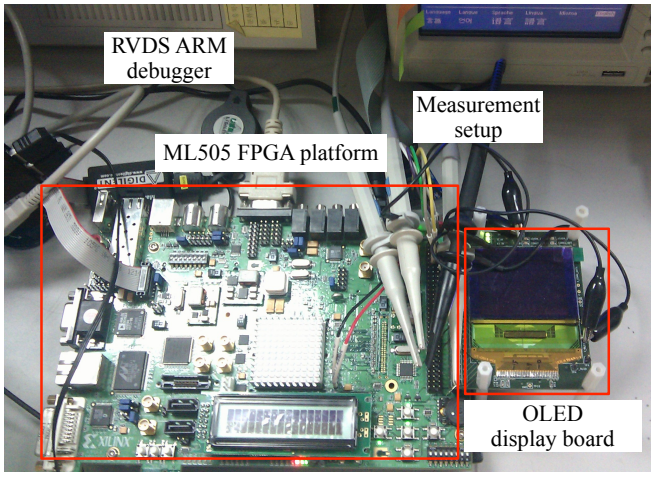


Fig. 18. Experimental setup for the OLED DVS with the prototype implementation.

sequence from a movie clip. Fig. 18 shows the experimental setup with the implemented prototype.

Fig. 19 summarizes the result for the still images. We capture the displayed images on the target OLED display panel by digital camera. The Lena and mandrill images have a typical balanced color distribution while the boat and

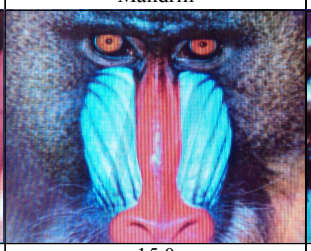
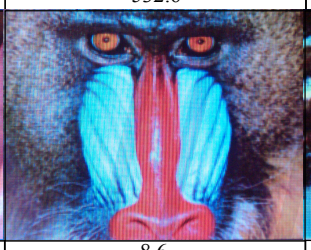
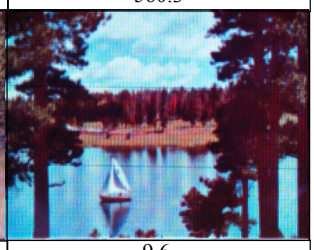
	Airplane	Lena	Mandrill	Boat
Displayed original images				
V_{DD} (V)	15.0	15.0	15.0	15.0
Power (mW)	731.7	399.9	532.6	560.3
Displayed scaled images				
V_{DD} (V)	12.0	8.7	8.6	9.6
Power (mW)	572.5	189.8	134.4	161.0
Saving (%)	21.8	52.5	74.7	71.3

Fig. 19. Photographs of the actual image on the OLED panel in PWM driver equipped prototype with standard test images.

airplane images have a severe skew toward the bright colors, which is challenging for the OLED DVS. The originally high luminance pixels are saturated to the maximum luminance as shown in the compensated images and histograms. The saturated pixels result in the image distortion, but the overall image quality is not appreciably altered within the threshold value.

The Lena image shows 52.5% power saving compared with the original image while V_{DD} being scaled down from 15 V to 8.7 V and with nearly zero color distortion. The mandrill image shows 74.7% power saving while V_{DD} being scaled down from 15 V to 8.6 V and with 300 as the average distortion. The boat image shows 71.3% power saving V_{DD} being scaled down from 15 V to 9.6 V and with 300 as the average distortion. As for the worst case among the benchmarks, the airplane still exhibits 21.8% power saving compared to the original image with 15 V V_{DD}.

We measure the display power consumption while playing the same movie clip in Section VII-A to evaluate the prototype and SoC. As shown in Fig. 20, the original movie clip with a 15 V V_{DD} shows 7.44 J energy consumption during 10 s, and a movie clip with a 5% distortion constraint shows 4.77 J. We confirm that V_{DD} is more aggressively scaled with larger distortion threshold in Fig. 20.

VIII. Conclusion

Organic light emitting diode (OLED) panels are promising display devices capable of self-illumination and thus exhibiting high power efficiency. However, OLED panel consumes comparable amount of power to liquid crystal display (LCD) due to serious total internal reflection. All previous OLED power saving methods change the pixel colors since the pixel color determines the OLED power consumption. Unfortunately, these methods result in significant degradation of the image.

This paper presents the OLED power saving method that enables only minimal pixel distortion, small enough to work with natural images. Furthermore, the proposed technique can be applied to most OLED panel structures. We developed such a unique power saving technique based on a careful analysis of the OLED driver architectures. The proposed method is called OLED dynamic voltage scaling (OLED DVS). We scale down the supply voltage and, in turn, dramatically reduce the wasted power caused by the voltage drop across the driver transistor as well as internal parasitic resistance. The proposed OLED DVS may incur image distortion after the supply voltage scaling. In this case, we compensate the image data based on the human-perceived color space.

We present a simulation result for the OLED panel with the AM driver circuit. We implemented a prototype with the PWM driver equipped-panel and demonstrate the OLED DVS. We demonstrated the OLED DVS for the still images with a prototype implementation and confirmed a 74.7% power saving for the Lena image with virtually zero distortion. We also measure the power saving of the OLED DVS for the sample movie clips by the using the prototype, and confirm up to 35.9% display power saving in average with 0.7% power and 7.7% slice overhead on the prototype implementation.

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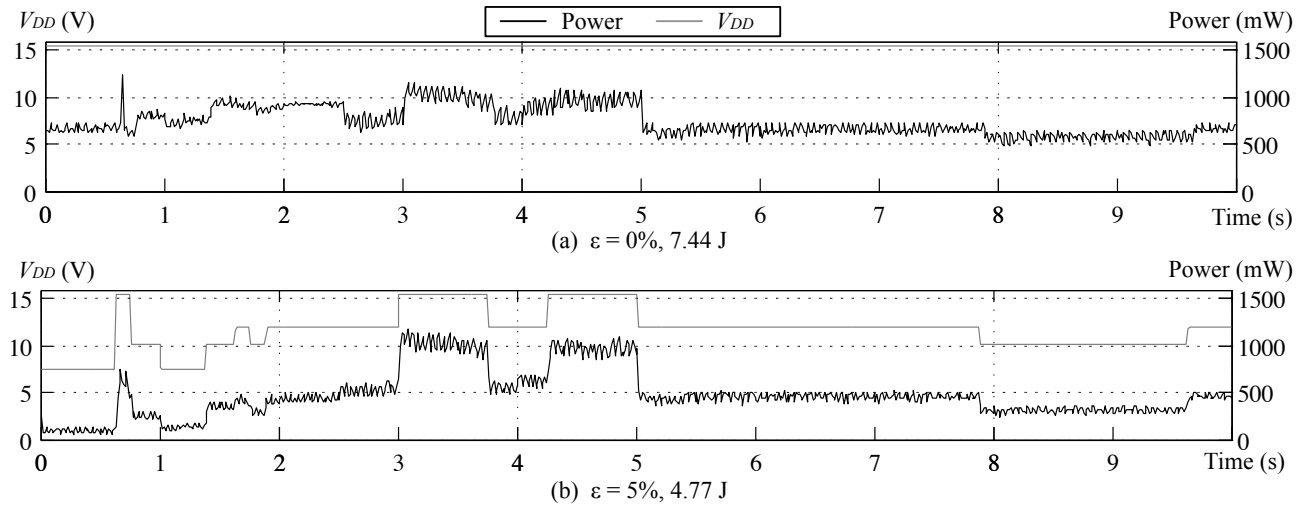

Fig. 20. Measured power consumption with OLED DVS for the movie clips with (a) 0% distortion tolerance (b) 5% distortion tolerance

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