Low Power DCVSL Circuits Employing AC Power Supply*

Xunwei Wu
Institute of Circ. and Syst.
Ningbo Univ., Ningbo
315211, CHINA
xunweiwu@mail.hz.zj.cn

Guoqiang Hang
Dept. of Info. and Elec. Eng.,
Zhejiang Univ., Hangzhou
310027, CHINA
hanggq@mail.hz.zj.cn

Massoud Pedram
Dept. of Elec. Eng.-Systems
University of Southern California
Los Angeles, CA 90089
pedram@ceng.usc.edu

*This project was sponsored in part by NNSF of China (Grant No.69973039) and NSF of USA (Grant No. 9988441).

Abstract. *In view of changing the type of energy conversion in CMOS circuits, this paper investigates low power CMOS circuit design, which adopts a gradually changing power clock. First, we discuss the algebraic expressions and the corresponding properties of clocked power signals. Then the design procedure is summed up for converting complementary CMOS logic gates employing DC power to the power-clocked CMOS gates employing AC power. On this basis, the design of differential cascode voltage switch logic (DCVSL) circuits employing AC power clocks is proposed. The PSPICE simulations using a sinusoidal power-clock demonstrate that the designed power-clocked DCVSL circuit has a correct logic function and low power characteristics. Finally, an interface circuit to convert clocked signals into the standard logic levels of a CMOS circuit is proposed, and its validity is verified by computer simulations.*

Keywords: VLSI design, low power technique, AC power, clocked DCVSL circuit.

1 Introduction

With the development of CMOS technology, the increasing scale and speed of integrated circuits cause a dramatic increase in power dissipation. The power dissipation of some processors such as Pentium, Alpha 21064, and Alpha 21164 has reached 16W, 30W, and 50W respectively. Low power technique has become an important research issue in VLSI design.

The power dissipation in CMOS circuits is related to the type of energy conversion present. In static CMOS circuits, a DC power supply is used and switching signal values are realized by charging and discharging the node capacitance. During this process, the charge is drawn from the power supply VDD, then transported to the node capacitance and returned to the ground terminal, resulting in an irreversible energy conversion from electric energy to heat. As a result, when a node capacitance is charged (or discharged), it leads to an energy dissipation of $(1/2)CV_{DD}^{2}$.[1] Thus reducing the energy dissipation has been equated to reducing the switching activity. Low power design targeting minimum switching activity has made significant progress in recent years.[2] However, the energy saving obtained is still limited.

Energy conversion is needed to represent a change in signal value. If energy exists only in one form, i.e., electric energy, then there is only one irreversible energy conversion from electric energy to heat. To break this one-way conversion, researchers have introduced another energy form, i.e., magnetic field energy, into the digital circuit. If one relates the signal change to the conversion of electric energy to magnetic energy, the so-called “energy-recovery” can be realized, by which the irreversible conversion from electric energy to heat caused by dissipative elements, i.e., resistors, is largely reduced.

The energy conversion from electric field to magnetic field and vice versa implies that circuits should be supplied with AC power. In this case, signals in the circuits should also be of alternating quantities. The latter has been used extensively in dynamic CMOS logic, clocked CMOS logic, and various Domino logics.[1] However, those circuits still rely on DC power, and the energy conversion remains an electric energy to heat conversion. Therefore, circuits supplied with AC power should be studied further. The AC power controls the working rhythm of the circuit and acts as the clock, so in this paper it will be called the “power-clock.” Research shows that if the a power clock with a gradually changing behavior is adopted, less energy is dissipated for charging and discharging the node capacitance through the conducting MOS transistor. Therefore, the so-called “adiabatic” switching operation is the result by which a new approach to design low power CMOS circuits is proposed.[3-11]

In Ref. [12] authors have introduced the idea that a gate and flip-flop design with the characteristic of energy recovery can be obtained based on traditional CMOS complementary logic gates by employing AC power. The research has been extended to design general low power circuits in Ref. [13]. In this paper the basic rules and circuit designs of combinational gates based on clocked CMOS transmission gate are discussed and differential cascode voltage switch logic circuits (DCVSL) are investigated by using AC power in order to supplement the family of CMOS circuits with energy recovery. PSPICE simulations prove that the designed circuits have a correct logic function and low power characteristics. Finally, an interface circuit to convert clocked signals into the logic levels of standard CMOS circuit is proposed, and its validity is verified by computer simulations.

2 Algebra for clocked signals

For the sake of simplicity, it is assumed that the clock used in this paper is a symmetric square-wave. When $clk = 1$, the clocked signal displays its true logic value; when $clk = 0$, the clocked signal is forced to its "base" value, 0 or 1. For the pre-charge circuits, the base value is 1 whereas for the pre-discharge circuits, the base value is 0. Therefore, in every clock cycle, the clocked signal is divided into two stages: set base (B) when $clk = 0$ and evaluate (E) when $clk = 1$.

Figure 1 shows a pair of complementary signals $x / \bar{x}$ and their corresponding clocked signals. The values of $x / \bar{x}$ in Fig.1 are (101101)/(010010); they can be regarded as the synchronous outputs of a falling-edge triggered-flip-flop. $x / \bar{x}$ are, however, not clocked signals. In Fig.2, $x^{\cdot clk}$, $\bar{x}^{\cdot clk}$, $x^{+\overline{clk}}$, and $\bar{x}^{+\overline{clk}}$ are four clocked signals derived from $x / \bar{x}$. Notice that the superscript i in the exponent expression of x^i, $i \in \{\cdot clk, +\overline{clk}\}$, represents the logic relation between the original signals $x / \bar{x}$ and the clocks $clk / \overline{clk}$. That is, $x^{\cdot clk}$ is $x \cdot clk$, $x^{+\overline{clk}}$ is $x + \overline{clk}$, and so on. Obviously, the function of $(\cdot clk)$ and $(+\overline{clk})$ is to set the clocked signal during the B stage to base 0 or base 1 respectively. In Figure1, we can find the difference in expressing logic values between general level signals and clocked signals: in the former, the logic values 1and 0 are expressed by the "high" and "low" of the level, respectively; whereas, in the latter, the logic values 1 and 0 are represented by the "presence" and "absence" of pulse, respectively.

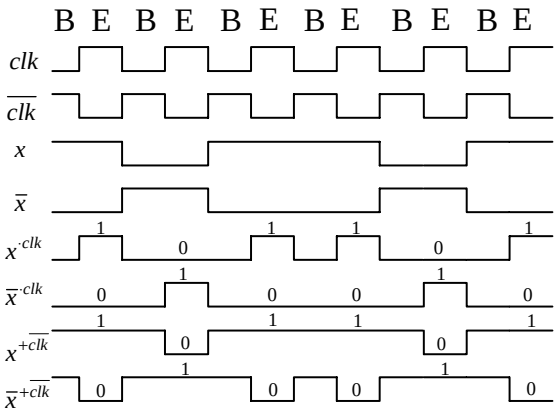


Fig.1 Four clocked signals derived from signal *x*

The following inverting relationships between the four clocked signals can be observed (cf. Fig.1):

1) Logical inverse (with the same base), such as $x^{\cdot clk}$ and $\overline{x}^{\cdot clk}$; $x^{+\overline{clk}}$ and $\overline{x}^{+\overline{clk}}$.
2) Base inverse (with the same logic value), such as $x^{\cdot clk}$ and $x^{+\overline{clk}}$; $\overline{x}^{\cdot clk}$ and $\overline{x}^{+\overline{clk}}$.
3) Complete inverse, such as $x^{\cdot clk}$ and $\overline{x}^{+\overline{clk}}$; $\overline{x}^{\cdot clk}$ and $x^{+\overline{clk}}$.

Figure 1 also shows that:

$$\overline{x^{\cdot clk}} = \overline{x}^{+\overline{clk}},\ \overline{\overline{x}^{\cdot clk}} = x^{+\overline{clk}}. \tag{1}$$

In line with the above-mentioned exponent expressions, the power supply V_{dd} (1), the ground (0) and the clock ($clk / \overline{clk}$) satisfy the following clocked expressions:

$$1 = 1^{+\overline{clk}},\ 0 = 0^{\cdot clk} \tag{2}$$

$$clk = 1^{\cdot clk}, \overline{clk} = 0^{+\overline{clk}} \tag{3}$$

If the exponent operation is regarded as a Boolean operation, then Eq.(2) and Eq.(3) can be easily proved. Furthermore, the following expressions can also be proven:

$$(x \cdot y)^{\cdot clk} = x^{\cdot clk} \cdot y^{\cdot clk},\ (x \cdot y)^{+\overline{clk}} = x^{+\overline{clk}} \cdot y^{+\overline{clk}} \tag{4}$$

$$(x + y)^{\cdot clk} = x^{\cdot clk} + y^{\cdot clk},\ (x + y)^{+\overline{clk}} = x^{+\overline{clk}} + y^{+\overline{clk}} \tag{5}$$

The physical meaning of the above Eq.(1) - Eq.(5) can be explained as follows:

1) Eq.(1) represents De Morgan's Law. It shows that the inverter function applied to clocked signals produces the complete inverse of the original clocked signals (i.e., both the logic value and the base are inverse).
2) Eq.(2) shows V_{dd} (1) and ground (0) can continually work in the clocked circuits of base 1 and base 0, respectively.
3) Eq.(3) indicates that clk can assume the role of power supply in the clocked circuit of base 0, whereas $\overline{clk}$ can assume the role of ground in the clocked circuit of base 1.
4) Eq.(4) and Eq.(5) suggest that the clocked signals that participate in the AND/OR operations should have the same base, and the result is equal to the original signals being ANDed/ORed together, then clocked by the same base. Furthermore the result of NAND and NOR operations inverts the base according Eq.(1).

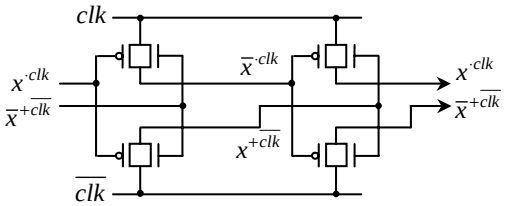
3 Complementary CMOS logic circuits employing AC power

Assuming that the basic circuits in clocked CMOS circuits are also the gates, the structure of clocked gates and their working principles are first investigated. Similar to the traditional CMOS gates, the outputs of the clocked CMOS gates should also be "restored." For traditional CMOS gates, the outputs are always clamped to either the power supply by a conductive pMOS transistor for the high-level output or the ground by a conductive nMOS transistor for the low-level output, whereby the level-restoration is realized.[14] Correspondingly, the outputs of the clocked CMOS gates should also be "clamped" to the power clock by a conductive MOS switch to obtain "pulse-restored" outputs. Because of the alternating characteristic of power clocks, this MOS switch should be the complementary CMOS transmission gate.

From the relationships among the four kinds of clocked signals shown in Figure 1, it can be seen that a pair of complete inverse clocked signals $x^{\cdot clk}$, $\overline{x}^{+\overline{clk}}$ can be used to control the pMOS and nMOS of the transmission gate respectively, and then the another pair of complete inverse clocked signals $\overline{x}^{\cdot clk}$, $x^{+\overline{clk}}$ can be generated when clk and $\overline{clk}$ are transmitted. On the other hand, the latter pair of clocked signals can be used to control the transmission of clk and $\overline{clk}$ to reproduce the former pair of clocked signals. From the above analysis, the circuit shown in Fig.2(a) can be derived. The relationships between the input and output in the circuit can be summed up as follows:

1) A pair of clocked signals used to control a transmission gate should be physically complementary. Among them, the base-0 and base-1 signal control the pMOS transistor and nMOS transistor respectively;
2) The output generated from clk is the base-0 signal and is the logic inverse to the input base-0 signal acting on the pMOS transistor. On the other hand, the output obtained from $\overline{clk}$ is a base-1 signal and is the logic inverse to the input base-1 signal acting on the nMOS transistor;
3) For any four unrestored clocked signal forms of a signal, its four restored clocked signals can be obtained by using two transmission gates to transmit power clocks clk and $\overline{clk}$.

(a)



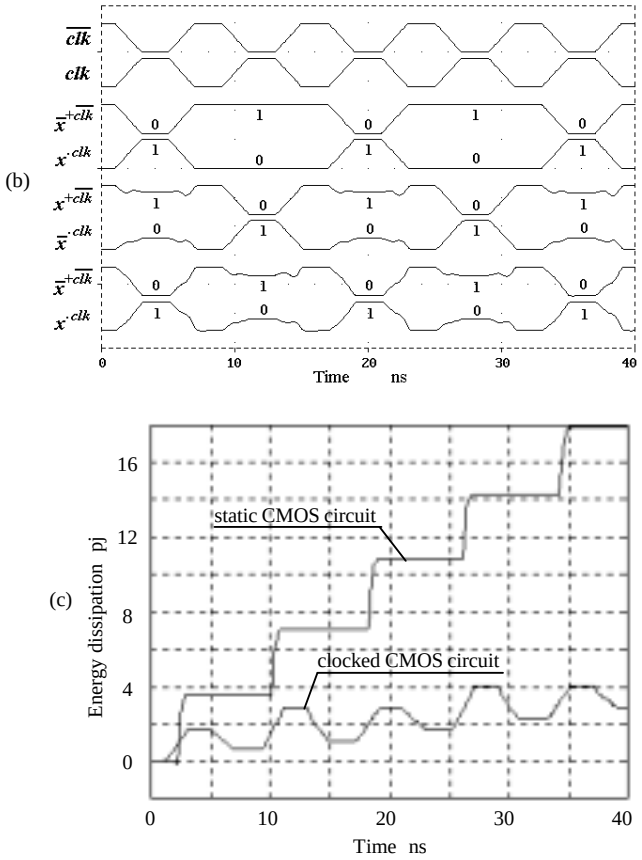


Fig.2 Power-clocked CMOS gate using a trapezoidal power-clock

(a) Circuit diagram, (b) Output waveforms, (c) Energy dissipation curve

By using a trapezoidal power-clock and the PSPICE program, the circuit in Figure 2(a) was simulated with 2μm CMOS technology. The result is given in Figure 2(b) where it can be seen that the output node signals do not maintain a flat high top or flat low bottom when the transmission gate shuts down. Taking $x^{+\overline{clk}}$ as an example, clk does not immediately jump to high-level when $x^{+\overline{clk}}$ is dropping. The nMOS transistor in the transmission gate is still turned-on at that moment, so the output tracks clk and rises until the nMOS transistor shuts down completely. However, the simulation has verified that these un-flat outputs do not affect the next stage. Figure 2(c) shows the energy dissipation curve of a one-stage circuit using a trapezoidal power-clock with a clocked input sequence pair (01010) and (10101). The decline part in the curve shows the effect of energy recovery. In contrast, we also draw the energy dissipation curve of the common two-stage inverter using DC power supply with the same conditions. It is shown that the former circuit has about 86% of energy saving in comparison with the latter. The power saving is remarkable.

Taking the inverter shown in Figure 3 as an example, the procedure by which a complementary CMOS logic gate employing DC power is converted to its counterpart employing AC power is illustrated. In Figure 3(b), (c), the structures with the CMOS transmission gate shown in Figure 2(a) have been redrawn in a form similar to the inverter shown in Figure 3(a) . The general conversion rules are as follows:

1) Tie both the supply terminal and the ground together and connect them to the same power clock *clk* (or $\overline{clk}$);

2) Both gates of the pMOS transistor and nMOS transistor are connected to two physically complementary clocked signals (a base-0 signal for pMOS transistor and a base-1 signal for nMOS transistor) rather than connected to the same input level signal.
3) The output is the logical complement of an input base-0 signal for a pMOS transistor if the power clock is *clk*; or, it is the logical complement of an input base-1 signal for an nMOS transistor if the power clock is $\overline{clk}$.

It should be pointed out that the above discussion in Figure3 is only for a simplest clocked inverter. In fact, by using the conversion rules we can realize NOR and NAND functions by connecting switches in series and parallel, and then the clocked CMOS circuits with more complicated logic function may be derived. [12,13]

Finally, we also notice that the signal types and transistor counts in the clocked circuits are doubled although the power dissipation is considerably decreased. For example, the signals used originally only have two polarities（$x, \overline{x}$）. However, current clocked signals have four polarities（$x^{\cdot clk}$, $\overline{x}^{\cdot clk}$ $x^{+\overline{clk}}$, and $\overline{x}^{+\overline{clk}}$）. Then the quadruple-rail inputs, rather than double-rail inputs, are needed for circuit synthesis. The circuit design will be more complicated.

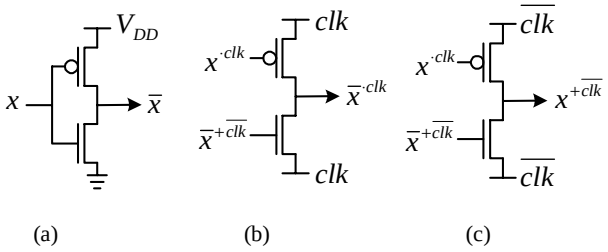


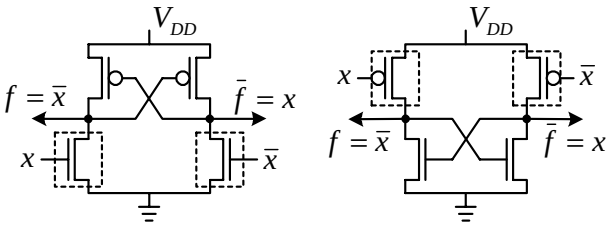
Fig.3 (a) Traditional inverter using DC power,
(b) Clock-powered inverter with a base-0 output signal,
(c) Clock-powered inverter with a base-1 output signal

4 DCVSL circuits with AC power

From the discussions in the previous section, it is found that the main drawback of the AC CMOS complementary logic circuits is that they perform their device count of circuit structure twice. However, the CMOS differential cascode voltage switch logic (DCVSL) employing DC power possesses complementary structure itself[15,16], which provides the possibility of enjoying the benefits of employing AC power without increasing the circuit complication.

The previously proposed DCVS inverter employing DC power is shown in Figure 4(a). In form, it has no advantages compared with the complementary logic inverter shown in Figure 3(a). However, in order to realize complicated logic function, the pMOS and the nMOS transistor of the inverter in Figure 3(a) should be replaced by a p-logic block and n-logic block respectively, but in the inverter of Figure 4(a), only the nMOS transistor should be replaced by the corresponding n-logic block. Therefore, the circuit structure of the latter is simpler than that of the former. Besides, the offered complementary logic outputs of the latter are simultaneous rather than a delay of one inverter. Though it is not proposed in References [15,16], with the exception of the

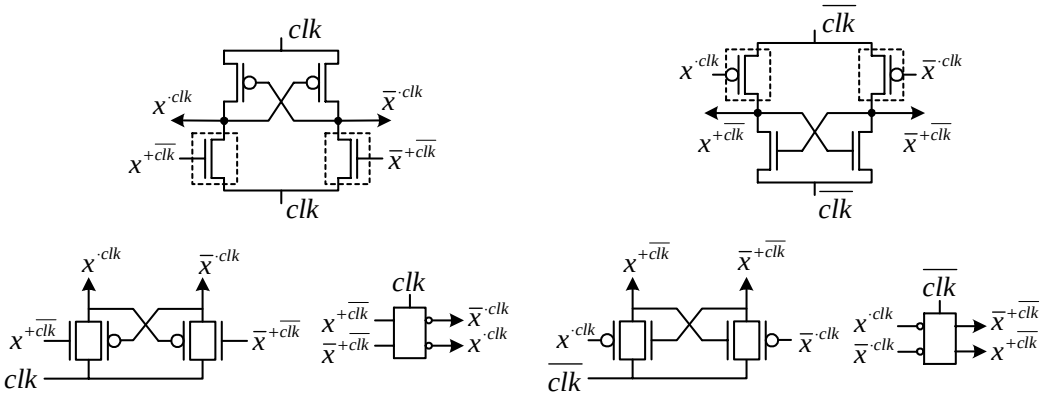
logic realization employing n-logic block corresponding to the Figure 4(a), another design employing p-logic block to realize logic functions also exists, as shown in Figure 4(b),.



(a) (b)

Fig.4 DCVSL circuits employing DC power, (a) n-logic (b) p-logic

According to the conversion rules summed up in the above section, on the basis of Figure 4, the design of a DCVS inverter employing AC power can be derived by conversion, as shown in Figure 5. If the power clocks in the two terminals are combined together, the corresponding structures assembled by CMOS transmission gates can be obtained. Their diagram symbols are also shown in Figure 5, where the signal line with a small circle denotes the input or output of the base-0 signal and those without a small circle denote the input or output of base-1 signal. Besides, the small circle is also used to express physical inverse between the input and the output.



(a) (b)

Fig.5 DCVSL circuits employing AC power (a) n-logic, (b) p-logic

Notice that the logic complementary inputs of the circuit shown in Figure 5(a) are base-1 signals, but its logic complementary outputs are all base-0 signals; whereas, the condition of the circuit shown in Figure 5(b) is just the reverse. Habitually, base-0 signals are adopted in the discussions of many references. Therefore, the circuit shown in Figure 5(b) is taken as the main body of logic circuits, and its base-1 output signals can be converted into base-0 signals again by connecting the inverter shown in Figure 5(a) in the output terminal, as shown in Figure 6(a). In the figure, if the pMOS transistor circled by the dotted line is replaced by a p-logic block, the complicated logic functions can be realized. As an example, the clocked DCVS AND/NAND gate and OR/NOR gate are shown in Figure 6(b) and Figure 6(c) respectively. Furthermore, in the following section, a full adder is used as an example to discuss the design of clocked DCVSL circuits with base-0 input and output signals.

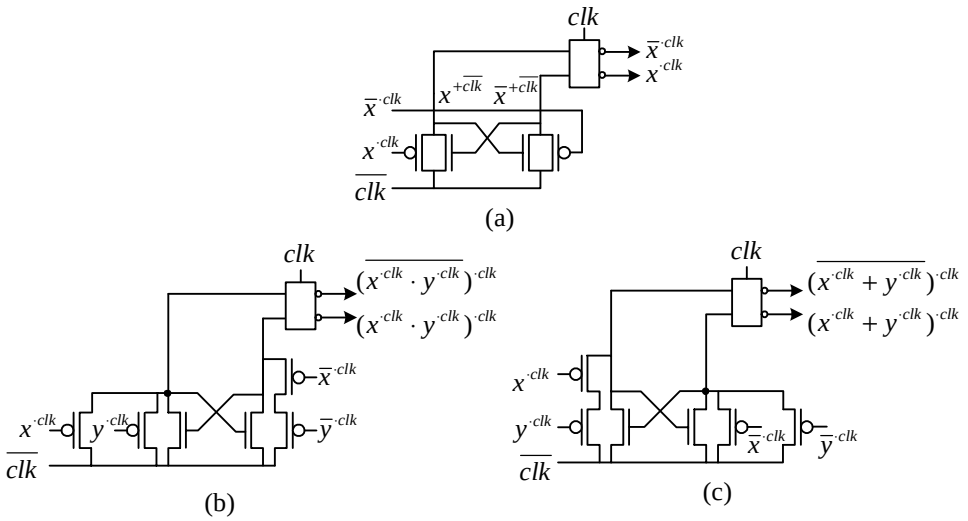
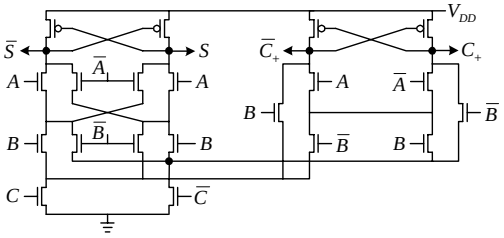
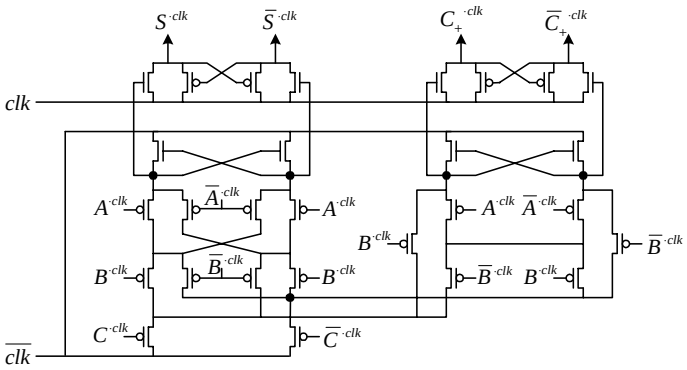


Fig.6 Basic power-clocked DCVSL gates with base-0 input/output signals

(a) Inverter/buffer, (b) AND/NAND gate, (c) OR/NOR gate

Reference [16] presented a DCVSL full adder operating on DC power. This circuit is shown in Figure 7(a). With the help of the conversion procedure described earlier, the corresponding power-clocked DCVSL full adder is derived and depicted in Figure 7(b). It is seen that only two additional "base-converting buffers" are required in comparison with the circuit shown in Figure 7(a). The circuit was simulated with PSPICE by using a sinusoidal power clock and with a Gray-coded 3-bit input stream. The input and output waveforms are shown in Figure 7(c). The energy dissipation waveform is also reported in Figure 7(d). These simulations demonstrate that the logic function of the power-clocked DVCSL circuit is correct and that there is clearly an energy recovery mechanism at work by which a considerable power saving is achieved. The circuit attains an energy savings of 95% compared to the design of DCVSL full adder employing DC power shown in Figure 7(a).





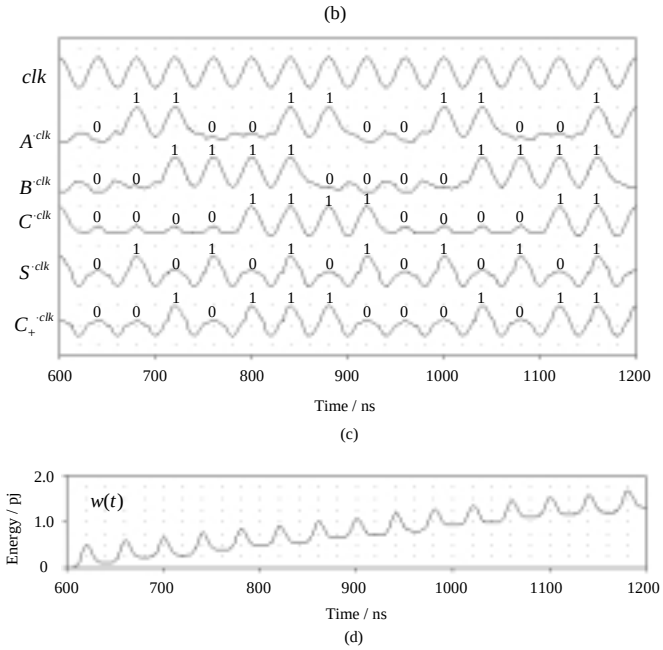


Fig.7 (a) DCVSL full adder using DC power , (b) DCVSL full adder using AC power, (c) PSPICE simulation with sinusoidal power clock, (d) Energy consumption waveform

In the discussions of Figure 1, it is implied that the general logic level signals can be converted into clocked signals by logic operations. In the following, the method to convert clocked signals into standard logic level signals will be investigated. One design scheme of an interface circuit is shown in Figure 8(a), which is constructed by one CMOS Schmitt inverter and a CMOS latch. The Schmitt circuit responds to a slowly changing clocked-signal with fast transition time at the output in order to reduce the simultaneous conducting time of both pMOS and nMOS transistors when connected with a static CMOS circuit (that is, the short circuit dissipation can be reduced). On the other hand, the Schmitt circuit has two threshold values: V_{T+} and V_{T-}, by which the drawback of run-up of low-level output signal can be effectively overcome when employing AC power. Therefore, the interference immunity of the circuit can be improved. In base-0 clocked circuits, when $clk = 0$, the clocked signal is set to its "base" value; when $clk = 1$, the clocked signal displays its true logic value; whereas, the condition of base-1 circuit is just the reverse. Therefore, the true logic value of the clocked signal can be sampled and latched in order to realize standard logic output. The clock of the latch is a pulse signal (ϕ), which has the same frequency as the power clock. For a base-0 clocked signal, it is sampled at the high level of the clock, and is latched at the low level of the clock. Whereas, the condition of the base-1 clocked signal is just the reverse. The proposed clocked DCVSL full adder is taken as an example. The clocked base-0 sum output signal ($S^{\cdot clk}$)and carry-out signal($C_+^{\cdot clk}$) are shown in Figure 7(b). If they act as the input signal of the interface circuit shown in Figure 8(a), the standard CMOS logic signals (sum output signal S and carry-out signal C_+) obtained from the PSPICE simulation, are shown in Figure 8(b). This result indicates that the output of the proposed DCVSL full adder employing AC power can drive standard static CMOS circuits by means of an interface circuit. Therefore, the application of the DCVSL full adder employing AC power is

further demonstrated.

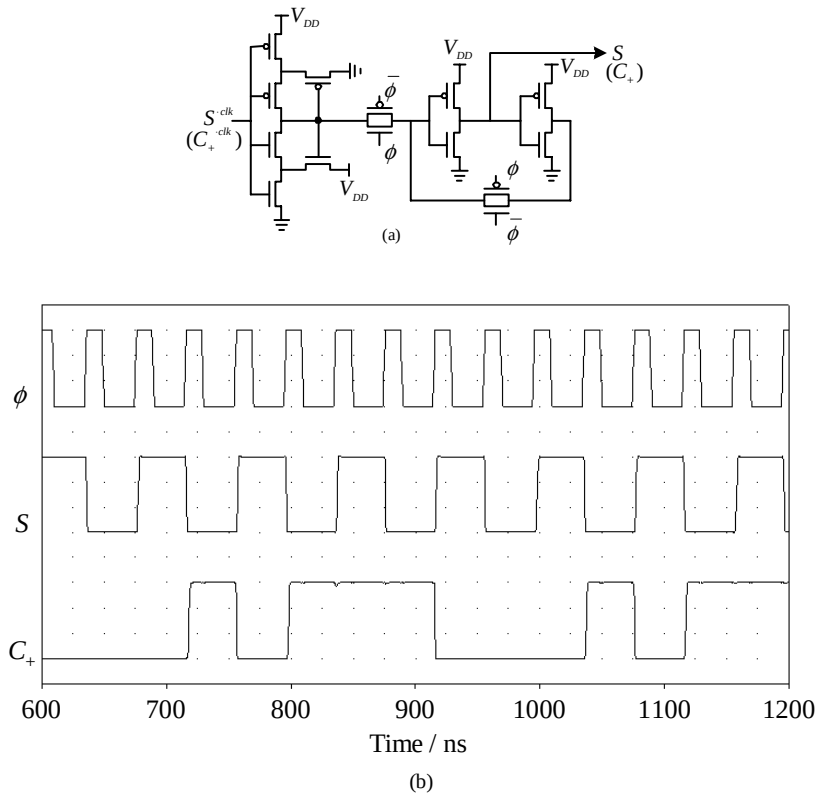


Fig.8 (a) The interface circuit between clocked CMOS and static CMOS circuits, (b) Converted static logic levels of a full adder

5 Conclusions

Clocked CMOS circuits, which employ a gradually rising and falling power clock, can result in a considerable energy saving. However, the demand that the output signal should track the power clock's gradually rising and falling behavior during charging and discharging makes the circuit design difficult. At present, the existing research either adopts retractile cascade power clocks or uses multiple phase power clocks with memory schemes in the design.[17,18] The problem is that the applicability of the designed clocked circuits is awfully limited. Thus the algebraic expression of clocked signals and the design of basic clocked gates are two key areas of research. Therefore, this paper presents a systematic study of clocked signals using appropriate algebraic expressions and fully exploits the four types of clocked signal. Furthermore, some clocked CMOS gate circuits based on a transmission gate are proposed. After comparing the clocked CMOS circuits with the traditional complementary logic CMOS circuits, the basic rules are summed up based on the conversion procedure from the complementary CMOS logic gates employing DC power to the clocked CMOS gates employing AC power (power clock). By using these rules the design of DCVSL circuits employing a power clock is proposed further. The circuit has an input and output with a convenient base-0 signal form, and its structure is not very complicated. By using a sinusoidal power clock the PSPICE simulations prove that the designed clocked DCVSL circuit has an ideal logic function and considerable power savings. To take the greatest advantage of the ultra-low power dissipation of CMOS circuits employing AC power and the characteristics of high speed and good interference immunity of static CMOS circuits, an interface circuit that is used to convert clocked signal into standard CMOS logic level is proposed. The validity of the interface circuit is verified by computer

simulation. Additionally, it is proved that the proposed DCVSL full adder employing AC power can be used in low power VLSI systems.

Finally, it should be pointed out that the main objective of a CMOS circuit employing AC power is to achieve low power design. The working frequency of the CMOS circuits employing AC power is determined by power clock. Therefore, to improve the speed of the circuit, the frequency of the power clock should be increased accordingly. Furthermore, the process of charging and discharging the node capacitance exits in CMOS circuits employing both AC power and DC power. However, in an AC powered circuit, the node level is not charged to the maximum power level or discharged to the minimum power level, as is the case in a DC-powered CMOS circuit. Therefore, in a high-speed CMOS circuit employing AC power, technology may be improved to reduce the node capacitance in order to complete the charging and discharging processes within one clock period.

References

[1] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, 2nd ed. New York: Addison - Wesley, 1993.

[2] M. Pedram, "Power minimization in IC design: principles and applications," *ACM Transactions on Design Automaton of Electronic Systems*, 1(1): 3-56, January 1996.

[3] W. C. Athas, L. J. Svensson, J. G. Koller, et al., "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. on VLSI Systems*, 2(4): 398-407, December 1994.

[4] J. S. Denker, "A review of adiabatic computing," in *Proc. of the Symposium on Low Power Electronics*, 1994, pp. 94-97.

[5] J. S. Denker, S. C. Avery, A. G. Dickinson, et al., "Adiabatic computing with the 2N-2N2D logic family," in *Proc. of the International Workshop on Low Power Design*, 1994, pp. 183-187.

[6] A. G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," *IEEE J. of Solid-State Circuits*, 30(3): 311-315, March 1995.

[7] A. Kamer, J. S. Denker, B. Flower, et al., "2ND order adiabatic computation with 2N-2P and 2N-2N2P logic circuits," in *Proc. of the International Symposium on Low Power Design*, 1995, pp. 191-196.

[8] D. Maksimovic, V. C. Oklobdzija, B. Nikolic, et al., "Clocked CMOS adiabatic logic with integrated single-phase power-clock supply: experimental results," in *Proc. of the International Symposium on Low-Power Electronics and Design*, 1997, pp. 323-327.

[9] V. C. Oklobdzija, D. Maksimovic, and F. Lin, "Pass-transistor adiabatic logic using single-clock supply," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10): 842-846, October 1997.

[10] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. of Solid-State Circuits*, SC-31(4): 514-522, April 1996.

[11] S. Kim and M. C. Papaefthymiou, "True single-phase-recovering logic for low-power, high-speed VLSI," in *Proc. of the International Symposium on Low-Power Electronics and Design*, 1998, pp. 167-172.

[12] X. Wu and M. Pedram, "Low power CMOS circuits with alternative power supply," in *Proc. China Eleventh Conference on Integrated Circuits and Silicon Materials* (in Chinese), 1999, pp. 688-691.

[13] M. Pedram and X. Wu, "Analysis of power-clocked CMOS with application to the design of energy-recovery circuits," in *Proc. of ASP-DAC*, 2000, pp. 339-344.

[14] X. Wu, "Theory of transmission switches and its application to design of CMOS digital circuits," *Int. J. of Circuit Theory and Application*, 20(4): 349-356, 1992.

[15] L. G. Heller, W. R. Griffin, J. W. Davis, and N. G. Thoma, "Cascode voltage switch logic: a differential CMOS logic family," in *Proc. Int. Conf. on Solid-State Circuits*, 1984, pp. 16-17.

[16] K. M. Chu and D. L. Pulfrey, "A comparison of CMOS circuit technique: differential cascode voltage switch logic versus conventional logic," *IEEE J. of Solid-State Circuits*, SC-24: 779-786, 1987.

[17] X. Wu and G. Hang, "Principle of adiabatic computing and CMOS circuits with energy recovery," *Chinese J. Computers* (in Chinese), 23(7): 779-785, July 2000.

[18] X. Wu and G. Hang, "Energy recovery circuits with cross-coupled structure," *J. of Circuits and Systems* (in Chinese), 5(2), 1-8, 2000.